Application Note

Anritsu

TD-SCDMA test

MG3700A
Vector Signal Generator

Application Note
- TD-SCDMA Test -

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MG3700A

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March 2007
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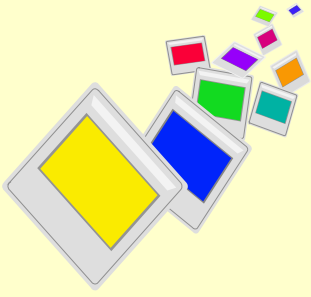
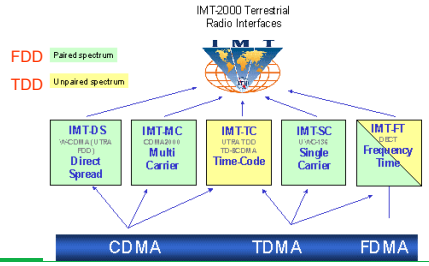
Contents



What is TD-SCDMA?

- TD-SCDMA (Time Division Synchronous Code Division Multiple Access) is one of the five IMT-2000 standards accepted by the ITU.
- The radio access interface of the UMTS (UTRA) comprises two standards for operation in the FDD and TDD modes.
- 3GPP standardizes three systems:
  - » *W-CDMA* UTRA FDD
  - » *TD-CDMA* UTRA TDD-HCR (High Chip Rate / Higher Chip Rate)
    - 3.84 Mcps, 5 MHz bandwidth / 7.68 Mcps, 10 MHz bandwidth
  - » *TD-SCDMA* UTRA TDD-LCR (Low Chip Rate)
    - 1.28 Mcps, 1.6 MHz bandwidth



UTRA/TDD Frequency Bands

Operating Band	Bandwidth [MHz]	Uplink/Downlink [MHz]	
a	20 + 15	1900 – 1920 2010 – 2025	China
b	60 + 60	1850 – 1910 1930 – 1990	
c	20	1910 – 1930	
d	50	2570 – 2620	

HSPA Standardization in 3GPP

- HSDPA (High-speed Downlink Packet Access) was standardized in 3GPP Release 5.
  - » The downlink peak data rate will increase to 2.8 Mbps.
  - » HS-DSCH
    - – HARQ for downlink
    - – Fast BTS downlink scheduling
    - – Shorter downlink TTI
    - – Higher order and adaptive modulation

HSDPA UE Capabilities (Categories)

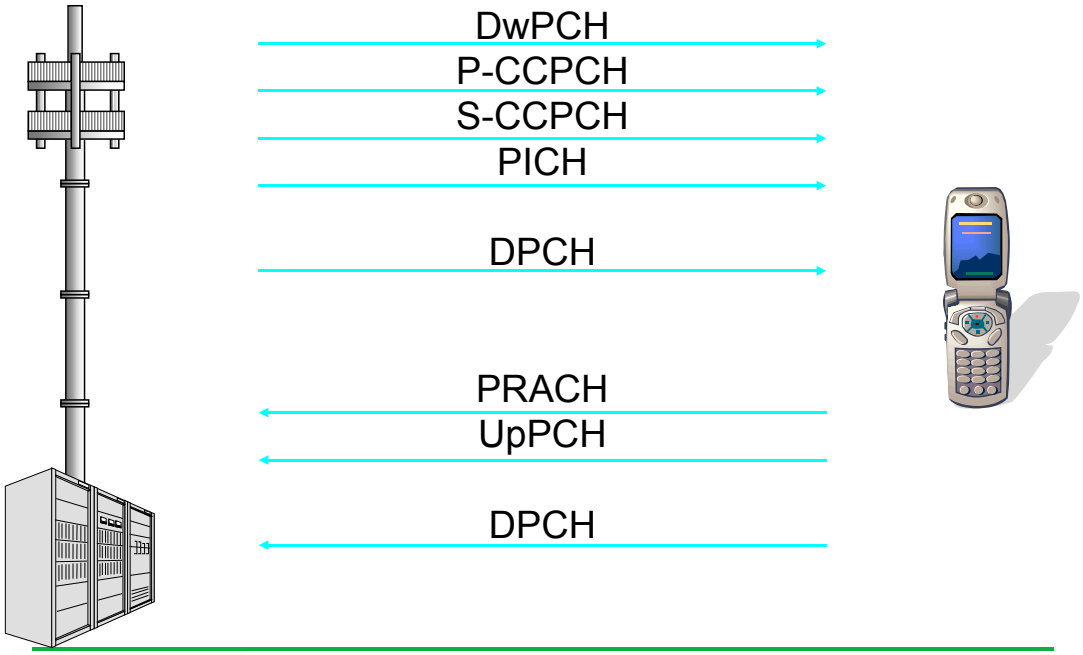
- 3GPP TS 25.306 specifies UE capabilities for HS-DSCH categories.

Category	Maximum Number of HS-PDSCH Codes per Timeslot	Maximum Number of HS-PDSCH Timeslots per TTI	Maximum Number of Transport Channel Bits per HS-DSCH TTI	Achievable Maximum Data Rate [Mbps]
1	12	5	7008	1.4
2	12	5	7008	1.4
3	12	5	7008	1.4
4	16	5	7008	1.4
5	16	5	7008	1.4
6	16	5	7008	1.4
7	12	5	10204	2
8	12	5	10204	2
9	12	5	10204	2
10	16	5	10204	2
11	16	5	10204	2
12	16	5	10204	2
13	16	5	14034	2.8
14	16	5	14034	2.8
15	16	5	14034	2.8

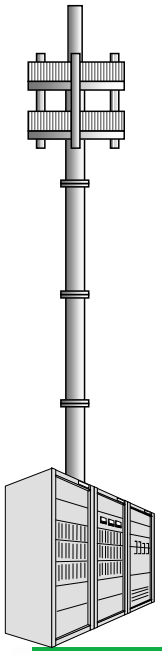
Mapping of Transport Channels onto Physical Channels

Transport Channels	Physical Channels	
– DCH	– DPCH	Dedicated Physical Channel
– BCH	– P-CCPCH	Primary Common Control Physical Channel
– PCH	– S-CCPCH	Secondary Common Control Physical Channel
– FACH	– PICH	Paging Indicator Channel
	– MICH	MBMS Indication Channel
	– PLCCH	Physical Layer Common Control Channel
– RACH	– PRACH	Physical Random Access Channel
– USCH	– PUSCH	Physical Uplink Shared Channel
– DSCH	– PDSCH	Physical Downlink Shared Channel
	– DwPCH	Downlink Pilot Channel
	– UpPCH	Uplink Pilot Channel
	– FPACH	Fast Physical Access Channel
HSDPA – HS-DSCH	– HS-PDSCH	High Speed Physical Downlink Shared Channel
	– HS-SCCH	Shared Control Channel for HS-DSCH
	– HS-SICH	Shared Information Control for HS-DSCH

Basic Physical Channels



HSDPA Physical Channels



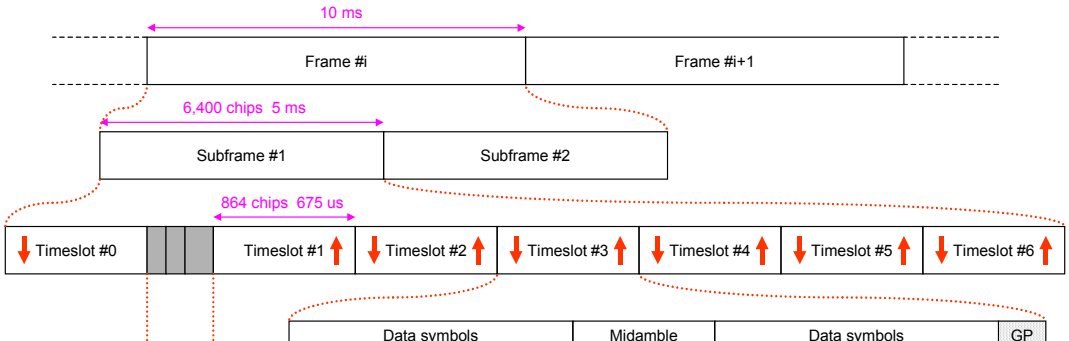
HS-SCCH

HS-PDSCH

HS-SICH

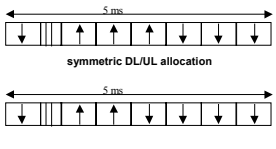
(DPCH)

Frame, Burst



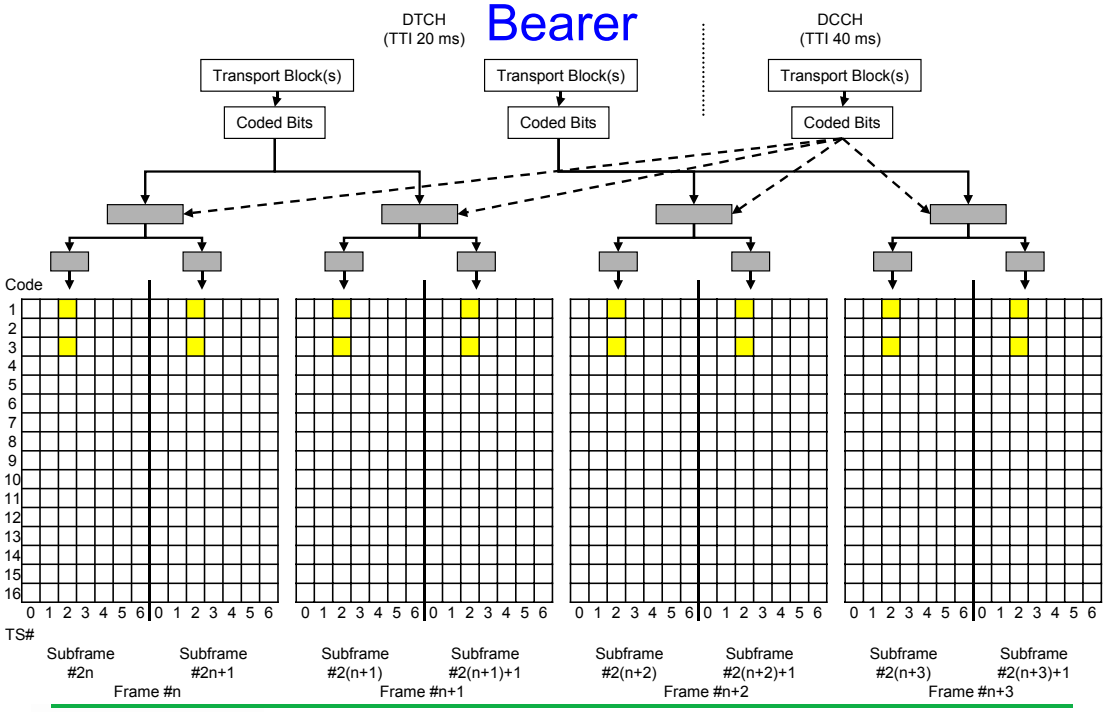
Spreading factor (Q)	Number of symbols (N) per data field in Burst
1	352
2	176
4	88
8	44
16	22

- Example



- DwPTS: Downlink Pilot Time Slot
- UpPTS: Uplink Pilot Time Slot
- GP: Guard Period

Mapping of Transport Blocks onto Physical Bearer



Downlink Physical Channels

- Common Channels
  - » *DwPCH* is a synchronization channel that is equal to the *DwPTS*. It is transmitted at each subframe with an antenna pattern configuration which provides whole cell coverage. Furthermore it is transmitted with a constant power level that is signalled by higher layers. The *SYNC_DL* code is not scrambled.
  - » *P-CCPCH* and *S-CCPCH* are common physical channels intended for carrying system and cell information and messages for UEs when a dedicated channel is not in place for communication.
  - » *PICH* is a channel that exists only at the physical layer. It is used to notify UEs of the outstanding paging messages on the Paging Channel (PCH).

Downlink Physical Channels

- Common Channels
  - *FPACH* is used by BS to carry (in one burst) the acknowledgement of a detected signature with timing and power level adjustment indication to a UE. It uses of one code with SF 16, so its burst is composed of 44 symbols. The spreading code, training sequence, and timeslot position are configured by the network and signalled on the *BCH*.
  - *PDSCH* is a shared channel across all users requesting packet data services. Each cell may support one or more *PDSCH*s. The theoretical peak data rate is about 2 Mbps.
  - *MICH* is a physical channel used to carry the MBMS notification indicators. The UE may use multiple *MICH* within the MBMS modification period to make decisions about individual MBMS notification indicators.
    - MBMS: Multimedia Broadcast and Multicast Service

Downlink Physical Channels

- Common Channels
  - *HS-PDSCH* is a shared channel across all users requesting HSDPA specific high-speed packet data services. Each cell may support one or more *HS-PDSCH*s. Sharing of the *HS-PDSCH* is based on Time Division Multiplexing (TDM) across multiple users. It uses 16QAM modulation.
  - *HS-SCCH* is a control channel associated with *HS-PDSCH*. It conveys the *HS-PDSCH* allocation information, including the user identity, SF, and modulation scheme.
- Dedicated Channels
  - *DPCH* is the dedicated physical channel for transport of information between the network and UE using a dedicated link on the physical channel.

Uplink Physical Channels

- Common Channels
  - *UpPCH* is a synchronization channel that is equal to the *UpPTS*. It is sent by the UE. It is used for BS to determine the received power level and timing. The *SYNC_UL* code is not scrambled.
  - *PRACH* is shared by UEs. It is used for initial access of the system.
  - *PUSCH* is used to carry bursty traffic for packet transmission.
  - *HS-SICH* carries the feedback signalling related to downlink HS-DSCH (incoming packets). The HS-DSCH-related feedback signalling consists of Hybrid-ARQ Acknowledgement (HARQ-ACK) and Channel-Quality Indication (CQI).

Uplink Physical Channels

- Dedicated Channels
  - *DPCH* is the dedicated physical channel for transport of information between the network and UE using a dedicated link on the physical channel.

Timeslot Formats for Downlink QPSK

Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} code word (bits)	N_{SS} & N_{TPC} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field(1)}$ (bits)	$N_{data/data\ field(2)}$ (bits)
0	16	144	0	0 & 0	88	88	44	44
1	16	144	4	0 & 0	88	86	42	44
2	16	144	8	0 & 0	88	84	42	42
3	16	144	16	0 & 0	88	80	40	40
4	16	144	32	0 & 0	88	72	36	36
5	16	144	0	2 & 2	88	84	44	40
6	16	144	4	2 & 2	88	82	42	40
7	16	144	8	2 & 2	88	80	42	38
8	16	144	16	2 & 2	88	76	40	36
9	16	144	32	2 & 2	88	68	36	32
10	1	144	0	0 & 0	1408	1408	704	704
11	1	144	4	0 & 0	1408	1406	702	704
12	1	144	8	0 & 0	1408	1404	702	702
13	1	144	16	0 & 0	1408	1400	700	700
14	1	144	32	0 & 0	1408	1392	696	696
15	1	144	0	2 & 2	1408	1404	704	700
16	1	144	4	2 & 2	1408	1402	702	700
17	1	144	8	2 & 2	1408	1400	702	698
18	1	144	16	2 & 2	1408	1396	700	696
19	1	144	32	2 & 2	1408	1388	696	692
20	1	144	0	32 & 32	1408	1344	704	640
21	1	144	4	32 & 32	1408	1342	702	640
22	1	144	8	32 & 32	1408	1340	702	638
23	1	144	16	32 & 32	1408	1336	700	636
24	1	144	32	32 & 32	1408	1328	696	632

Timeslot Formats for Uplink QPSK

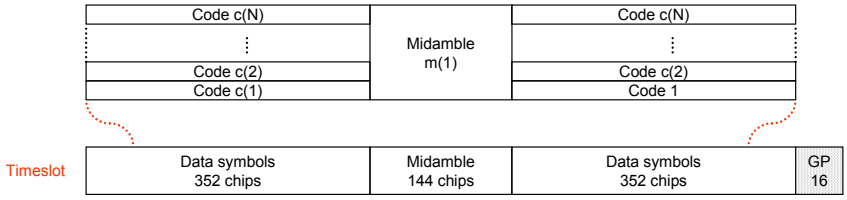
Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} code word (bits)	N_{SS} & N_{TPC} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field(1)}$ (bits)	$N_{data/data\ field(2)}$ (bits)
0	16	144	0	0 & 0	88	88	44	44
1	16	144	4	0 & 0	88	86	42	44
2	16	144	8	0 & 0	88	84	42	42
3	16	144	16	0 & 0	88	80	40	40
4	16	144	32	0 & 0	88	72	36	36
5	16	144	0	2 & 2	88	84	44	40
6	16	144	4	2 & 2	88	82	42	40
7	16	144	8	2 & 2	88	80	42	38
8	16	144	16	2 & 2	88	76	40	36
9	16	144	32	2 & 2	88	68	36	32
10	8	144	0	0 & 0	176	176	88	88
11	8	144	4	0 & 0	176	174	86	88
12	8	144	8	0 & 0	176	172	86	86
13	8	144	16	0 & 0	176	168	84	84
14	8	144	32	0 & 0	176	160	80	80
15	8	144	0	2 & 2	176	172	88	84
16	8	144	4	2 & 2	176	170	86	84
17	8	144	8	2 & 2	176	168	86	82
18	8	144	16	2 & 2	176	164	84	80
19	8	144	32	2 & 2	176	156	80	76
20	8	144	0	4 & 4	176	168	88	80
21	8	144	4	4 & 4	176	166	86	80
22	8	144	8	4 & 4	176	164	86	78
23	8	144	16	4 & 4	176	160	84	76
24	8	144	32	4 & 4	176	152	80	72
25	4	144	0	0 & 0	352	352	176	176
26	4	144	4	0 & 0	352	350	174	176
27	4	144	8	0 & 0	352	348	174	174
28	4	144	16	0 & 0	352	344	172	172
29	4	144	32	0 & 0	352	336	168	168
30	4	144	0	2 & 2	352	348	176	172
31	4	144	4	2 & 2	352	346	174	172
32	4	144	8	2 & 2	352	344	174	170
33	4	144	16	2 & 2	352	340	172	168
34	4	144	32	2 & 2	352	332	168	164
35	4	144	0	8 & 8	352	336	176	160
36	4	144	4	8 & 8	352	334	174	160
37	4	144	8	8 & 8	352	332	174	158
38	4	144	16	8 & 8	352	328	172	156
39	4	144	32	8 & 8	352	320	168	152
40	2	144	0	0 & 0	704	704	352	352
41	2	144	4	0 & 0	704	702	350	352
42	2	144	8	0 & 0	704	700	350	350
43	2	144	16	0 & 0	704	696	348	348
44	2	144	32	0 & 0	704	688	344	344
45	2	144	0	2 & 2	704	700	352	348
46	2	144	4	2 & 2	704	698	350	348
47	2	144	8	2 & 2	704	696	350	346
48	2	144	16	2 & 2	704	692	348	344
49	2	144	32	2 & 2	704	684	344	340
50	2	144	0	16 & 16	704	672	352	320
51	2	144	4	16 & 16	704	670	350	320
52	2	144	8	16 & 16	704	668	350	318
53	2	144	16	16 & 16	704	664	348	316
54	2	144	32	16 & 16	704	656	344	312
55	1	144	0	0 & 0	1408	1408	704	704
56	1	144	4	0 & 0	1408	1406	702	704
57	1	144	8	0 & 0	1408	1404	702	702
58	1	144	16	0 & 0	1408	1400	700	700
59	1	144	32	0 & 0	1408	1392	696	696
60	1	144	0	2 & 2	1408	1404	704	700
61	1	144	4	2 & 2	1408	1402	702	700
62	1	144	8	2 & 2	1408	1400	702	698
63	1	144	16	2 & 2	1408	1396	700	696
64	1	144	32	2 & 2	1408	1388	696	692
65	1	144	0	32 & 32	1408	1344	704	640
66	1	144	4	32 & 32	1408	1342	702	640
67	1	144	8	32 & 32	1408	1340	702	638
68	1	144	16	32 & 32	1408	1336	700	636
69	1	144	32	32 & 32	1408	1328	696	632

Timeslot Formats for Downlink and Uplink 8PSK

Slot Format #	Spreading Factor	Midamble length (chips)	N_{TFCI} code word (bits)	N_{SS} & N_{TPC} (bits)	Bits/slot	$N_{Data/Slot}$ (bits)	$N_{data/data\ field(1)}$ (bits)	$N_{data/data\ field(2)}$ (bits)
0	1	144	0	0 & 0	2112	2112	1056	1056
1	1	144	6	0 & 0	2112	2109	1053	1056
2	1	144	12	0 & 0	2112	2106	1053	1053
3	1	144	24	0 & 0	2112	2100	1050	1050
4	1	144	48	0 & 0	2112	2088	1044	1044
5	1	144	0	3 & 3	2112	2106	1056	1050
6	1	144	6	3 & 3	2112	2103	1053	1050
7	1	144	12	3 & 3	2112	2100	1053	1047
8	1	144	24	3 & 3	2112	2094	1050	1044
9	1	144	48	3 & 3	2112	2082	1044	1038
10	1	144	0	48 & 48	2112	2016	1056	960
11	1	144	6	48 & 48	2112	2013	1053	960
12	1	144	12	48 & 48	2112	2010	1053	957
13	1	144	24	48 & 48	2112	2004	1050	954
14	1	144	48	48 & 48	2112	1992	1044	948
15	16	144	0	0 & 0	132	132	66	66
16	16	144	6	0 & 0	132	129	63	66
17	16	144	12	0 & 0	132	126	63	63
18	16	144	24	0 & 0	132	120	60	60
19	16	144	48	0 & 0	132	108	54	54
20	16	144	0	3 & 3	132	126	66	60
21	16	144	6	3 & 3	132	123	63	60
22	16	144	12	3 & 3	132	120	63	57
23	16	144	24	3 & 3	132	114	60	54
24	16	144	48	3 & 3	132	102	54	48

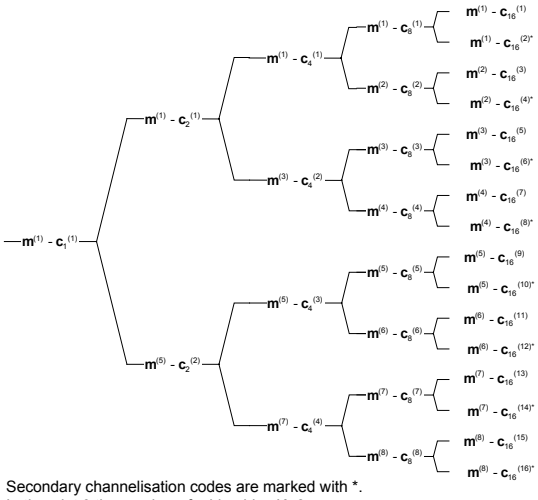
Midamble

- The data fields are separated by a midamble that is used for channel estimation.
  - » The midamble is used for both channel equalisation and coherent detection at the receiver. It reduces the user data payload.
- The scrambling code and basic midamble code are broadcast and may be constant within a cell.
  - » The same basic midamble code is used throughout the frame.
- The midambles, i.e. the training sequences of different users, are time-shifted versions of one periodic basic code. Different cells use different periodic basic codes, i.e. different midamble sets.



Midamble

- Association between Midambles and Channelisation Codes for K=8



Secondary channelisation codes are marked with *.
In timeslot 0 the number of midambles K=8.
In all of the other timeslot, K is individually configured from higher layers.

- Code Allocation

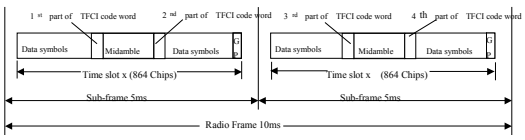
Code Group	Associated Codes			
	SYNC-DL ID	SYNC-UL ID	Scrambling Code ID	Basic Midamble Code ID
Group 1	0	0...7	0	0
			1	1
			2	2
			3	3
Group 2	1	8...15	4	4
			5	5
			6	6
			7	7
			.	
			.	
			.	
Group 32	31	248...255	124	124
			125	125
			126	126
			127	127

$m^{(k)}$ k: User number 1 to K; K: Maximum users 2, 4, 6, 8, 10, 12, 14, 16

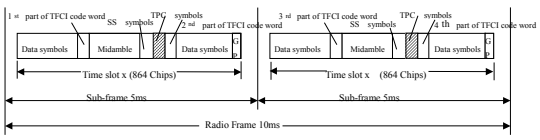
$c_Q^{(k)}$ k: Channelisation Code number 1 to Q; Q: SF 1, 2, 4, 8, 16

TFCI

- TFCI (Transmission Format Combination Indicator) is used to indicate the combination of used transport channels in DPCH and is sent only once per frame. TFCI uses in-band signalling and has its own coding. The number of TFCI bits is variable and is set at the beginning of the call.
- TFCI is always present in the first timeslot in a radio frame for each CCTrCH (Coded Composite Transport Channel).
  - » TFCI is transmitted in the data parts of the respective physical channel, meaning that TFCI code word bits and data bits are subject to the same spreading procedure.
  - » TFCI code word bits are equally distributed between the two subframes and respective data fields.



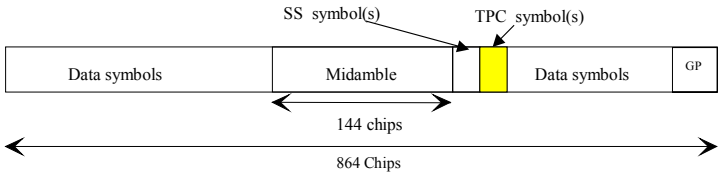
in case of no TPC and SS



in case of TPC and SS

TPC

- TPC (Transmitter Power Control) is transmitted in the data parts of the traffic burst in uplink and downlink.
- For every user, the TPC information is transmitted at least once per subframe.



- The length of the TPC command is one symbol.
  - TPC bit for QPSK

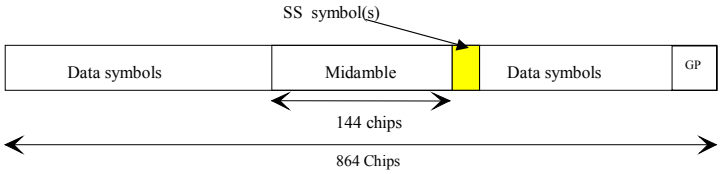
b_{TPC}	TPC command	Meaning
0	'Down'	Decrease Tx Power
1	'Up'	Increase Tx Power

  - TPC bit for 8PSK

TPC Bits	TPC command	Meaning
000	'Down'	Decrease Tx Power
110	'Up'	Increase Tx Power

SS

- SS (Synchronisation Shift) is transmitted in the data parts of the traffic burst in downlink and uplink.
- For every user, the SS information is transmitted at least once per transmitted subframe.
- SS is utilized to command a timing adjustment by k/8 × Tc.
  - Tc: 1.28 Mcps $^{-1}$ = 781.25 ns



- The length of the SS command is one symbol.
  - SS bit for QPSK

SS Bits	SS command	Meaning
00	'Down'	Decrease synchronisation shift by k/8 Tc
11	'Up'	Increase synchronisation shift by k/8 Tc
01	'Do nothing'	No change

  - SS bit for 8PSK

SS Bits	SS command	Meaning
000	'Down'	Decrease synchronisation shift by k/8 Tc
110	'Up'	Increase synchronisation shift by k/8 Tc
011	'Do nothing'	No change

BS Test

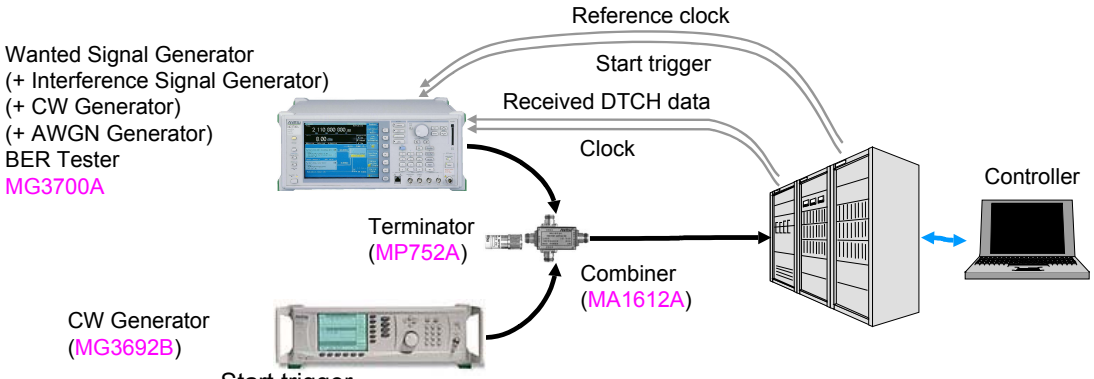
3GPP TS 25.142 (Release 7)
6 Transmitter
7 Receiver
8 Performance requirements

	Test	Wanted Signal Generator with BERT	Interference Signal Generator	CW Generator	AWGN Generator	Others
6.7	Transmit intermodulation		MG3700A			Spectrum Analyzer Circulator
7.2	Reference sensitivity level	MG3700A				
7.3	Dynamic range				*	
7.4	Adjacent Channel Selectivity (ACS)		*			
7.5	Blocking characteristics		*	MG3692B 20 GHz or MG3642A 2.08 GHz		MA1612A 3 GHz Combiner
7.6	Intermodulation characteristics		*			
8.2	Demodulation in static propagation conditions				*	
8.3	Demodulation of DCH in multipath fading conditions				MG3700A	MA1612A 3 GHz Combiner, Fading Simulator

*: MG3700A for the wanted signal generator generates two signals with interference signal, CW or AWGN.

Unsupported interference signal pattern
Unsupported HSPA

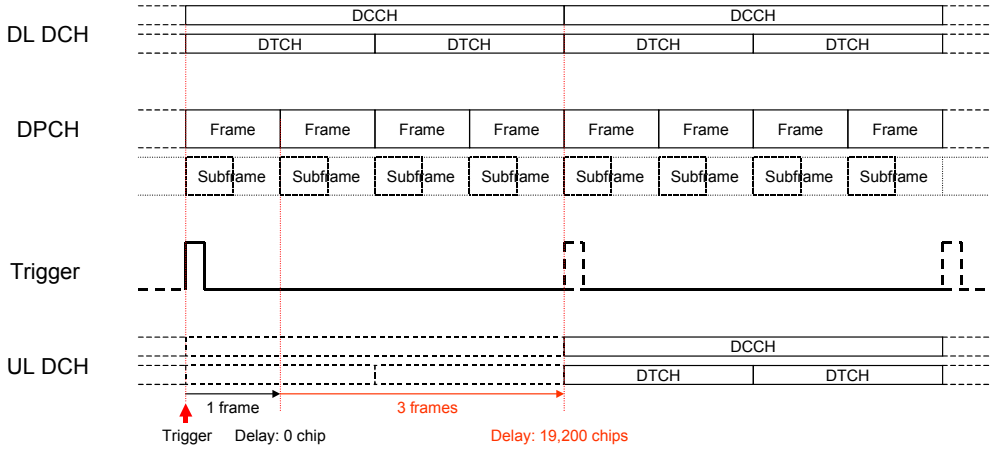
Receiver Test Setup Example



- Start trigger
  - Front panel [Start/Frame Trigger] Input
    - 40 ms × n clock
- Reference clock
  Use only one.
  - Rear panel [Baseband Ref Clock] Input
    - 1.28 MHz, 2 × 1.28 MHz (2.56 MHz), 4 × 1.28 MHz (5.12 MHz)
  - Rear panel [10MHz/5MHz Ref] Input
- Controller
  - Makes receivable state for UL RMC by FTM (Factory Test Mode) control
  - Reports internal BLER calculation for received DTCH

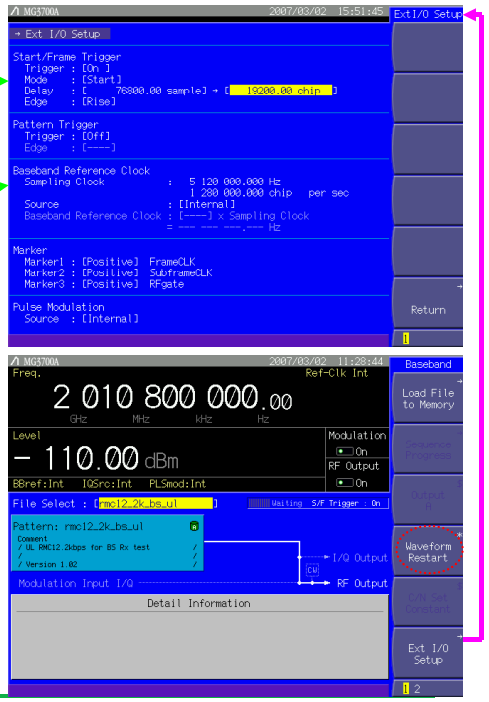
Timing Synchronization Setup Example

- Start trigger delay
  - » Set the timing at which the BS can receive UL RMC.



Timing Synchronization Setup Example

- Setting External Start trigger
  - » Captures/ Synchronizes trigger once only
- Reference clock
  - » [Baseband Ref Clock] Input usage case
    - – Source : [External]
    - – Baseband Reference Clock:
      - [1],[1/2],[1/4],[1/8],[1/16] ×
  - » [10MHz/5MHz Ref] Input usage case
    - – Source : [Internal]
- Trigger recapture/ synchronization



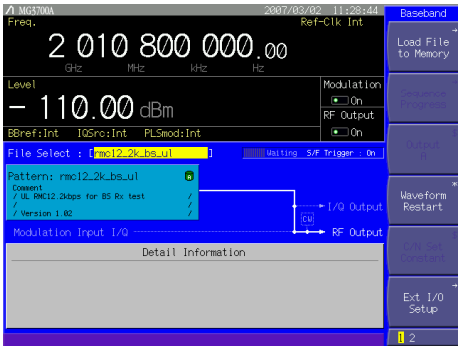
Scrambling Code Synchronization Setup Example

- Scrambling code
  - » Each basic midamble code is associated with a cell-specific complex scrambling code.
    - – Created from 16-bit long complex scrambling sequences
  - » Applies to scrambling (spreading)
- Set the scrambling code and basic midamble code to BS.
  - – 0

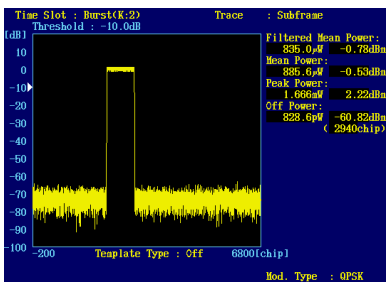
Code Group	Associated Codes			
	SYNC-DL ID	SYNC-UL ID	Scrambling Code ID	Basic Midamble Code ID
Group 1	0	0...7	0	0
			1	1
			2	2
			3	3
Group 2	1	8...15	4	4
			5	5
			6	6
			7	7
			.	
			.	
			.	
Group 32	31	248...255	124	124
			125	125
			126	126
			127	127

Wanted Signal Setup Example

Test
- Receiver
  excluding
  Dynamic range
- UL RMC 12.2 kbps



Setting power level is the Mean power.



Mean power is the power in a bandwidth of at least (1+α) times 1.28 MHz chip rate. The measurement period is a transmit timeslot excluding the guard period.

RRC filtered mean power is the power measured through a root raised cosine filter with roll-off α=0.22 and 1.28 MHz chip rate bandwidth.

For a perfectly modulated signal,
RRC filtered mean power = Mean power - 0.246 dB

Wanted Signal + Interference Signal Setup Example

Test
- ACS
- Blocking characteristics
- Intermodulation characteristics

- UL RMC 12.2 kbps

+

- Interferer
  - » Set Frequency offset.
    - -31.9872 ~ +31.9872 MHz

ACS: 1.6 MHz offset
Blocking: ≥ 3.2 MHz offset
Intermodulation: 6.4 MHz offset

Unsupported interference signal pattern

Interference Signal

The interference signal is equivalent to a continuous wideband CDMA signal with one code of chip frequency 1.28 Mcps, filtered by an RRC transmit pulse-shaping filter with roll-off α = 0.22.

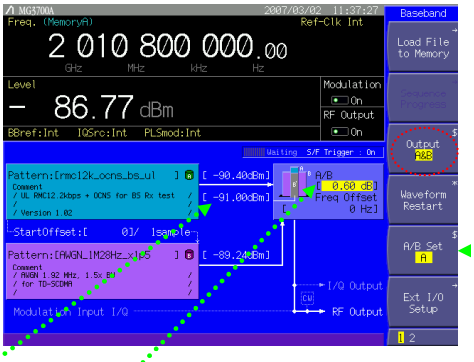
Wanted Signal + AWGN Setup Example

Test
- Dynamic range

- UL RMC 12.2 kbps
+
- AWGN

Test
- Performance requirements

- UL RMC 12.2 kbps
  - DPCHo multiplexing
- UL RMC 64 kbps
  - DPCHo multiplexing
- UL RMC 144 kbps
  - DPCHo multiplexing
- UL RMC 384 kbps
+
- AWGN
  - » Ioc [dBm/1.28MHz]



A/B Set	A level	B level	RF level
A	Variable	Static	Coupled
B	Static	Variable	Coupled
Constant	Variable	Variable	Static

Test Number	$\frac{\hat{I}_{or}}{I_{oc}}$ [dB]	BLER
1	0.6	10^{-2}
2	-0.9	10^{-1}
	-0.4	10^{-2}
3	-0.3	10^{-1}
	-0.1	10^{-2}
4	0.5	10^{-1}
	0.6	10^{-2}

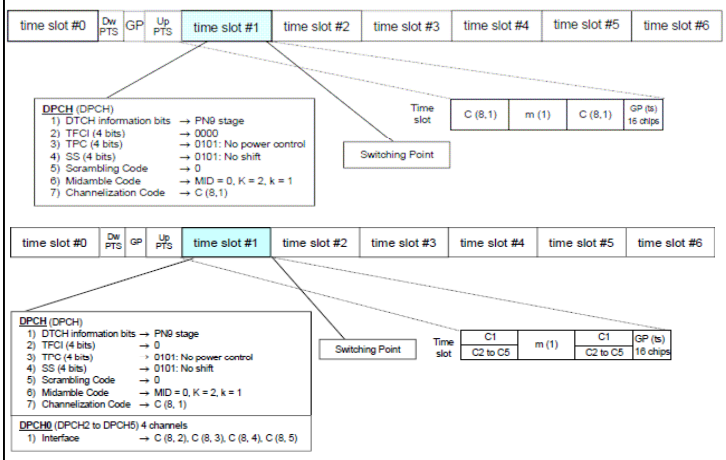
DPCHo

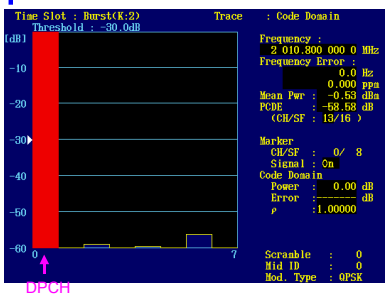
DPCHo simulates an individual intra-cell interferer that is equivalent to a valid UTRA TDD signal with SF 8, using the same time slot(s) as the wanted signal and applying the same cell-specific scrambling code.

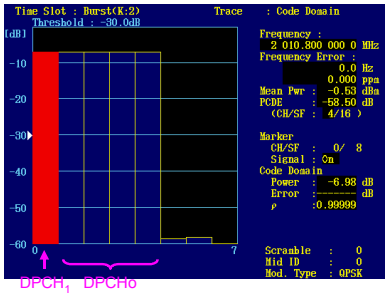
Parameters		Unit	Test 1	Test 2	Test 3	Test 4
Number of $DPCH_o$			4	1	1	0
Spread factor of $DPCH_o$			8	8	8	
$\frac{DPCH_o\_E_c}{I_{or}}$		dB	-7	-7	-7	–
I_{oc}	Wide Area BS	dBm/1,28 MHz	-91			
	Local Area BS	dBm/1,28 MHz	-77			
Information Data Rate		kbps	12,2	64	144	384

Test Number	BLER objective	Number of $DPCH_0$	Power of each $DPCH_0$ measured at the BS antenna connector [dBm]		Parameters of the wanted signal			
					DPCH	SF	Power measured at the BS antenna connector [dBm]	
			Wide Area BS	Local Area BS			Wide Area BS	Local Area BS
1	10^{-2}	4	-97.4	-83,4	$DPCH_1$	8	-97.4	-83,4
2	10^{-1}	1	-98.9	-84,9	$DPCH_1$	2	-92.9	-78,9
	10^{-2}	1	-98.4	-84,4	$DPCH_1$	2	-92.5	-78,5
3	10^{-1}	1	-98.3	-84,3	$DPCH_1$	2	-92.3	-78,3
	10^{-2}	1	-98.1	-84,1	$DPCH_1$	2	-92.1	-78,1
4	10^{-1}	0	–	–	$DPCH_1$	8	-97.5	-83,5
					$DPCH_2$	2	-91.5	-77,5
	10^{-2}	0	–	–	$DPCH_1$	8	-97.4	-83,4
					$DPCH_2$	2	-91.4	-77,4

UL RMC 12.2 kbps

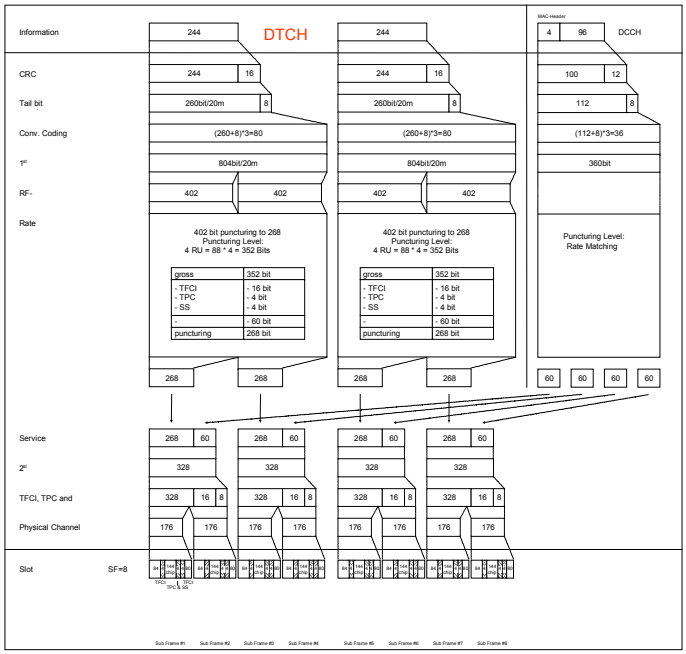




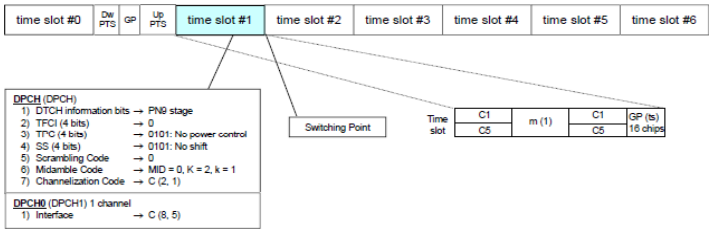


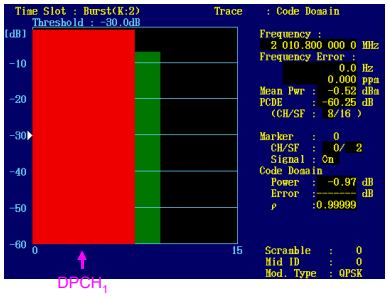
Parameter	Value
Information data rate	12.2 kbps
RU´s allocated	1TS (1*SF8) = 2RU/5ms
Midamble	144
Interleaving	20 ms
Power control	4 Bit/user/10ms
TFCI	16 Bit/user/10ms
Synchronisation Shift (SS)	4 Bit/user/10ms
Inband signalling DCCH	2.4 kbps
Puncturing level at Code rate 1/3 : DCH of the DTCH/ DCH of the DCCH	33% / 33%

UL RMC 12.2 kbps

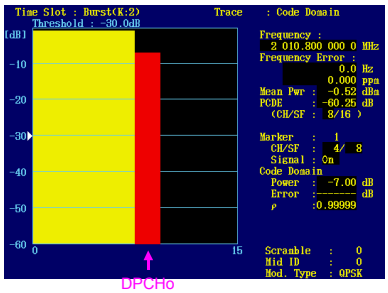


UL RMC 64 kbps

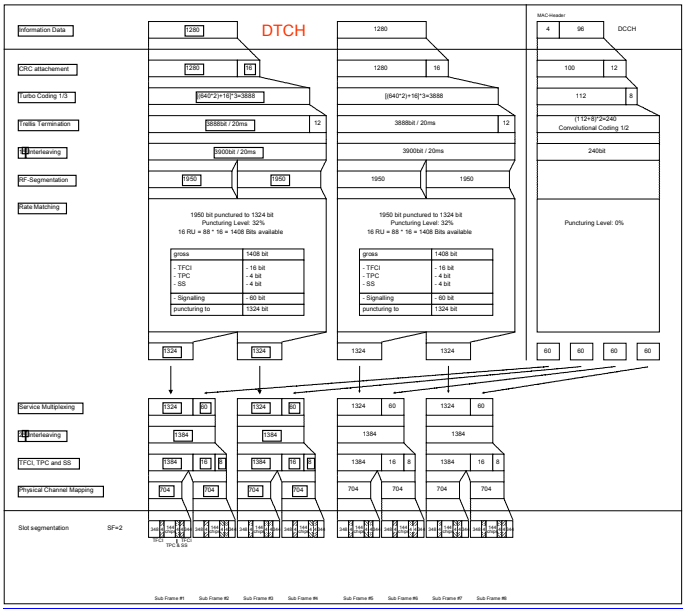




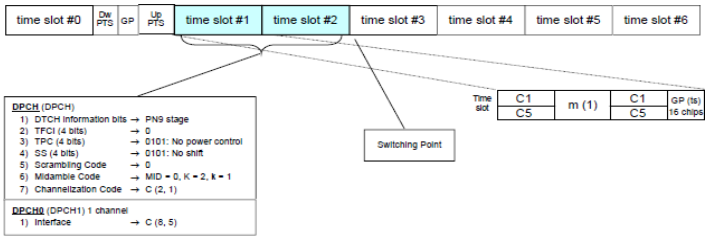
Parameter	Value
Information data rate	64 kbps
RU's allocated	1TS (1*SF2) = 8RU/5ms
Midamble	144
Interleaving	20 ms
Power control (TPC)	4 Bit/user/10ms
TFCI	16 Bit/user/10ms
Synchronisation Shift (SS)	4 Bit/user/10ms
Inband signalling DCCH	2.4 kbps
Puncturing level at Code rate: 1/3 DCH of the DTCH / ½ DCH of the DCCH	32% / 0

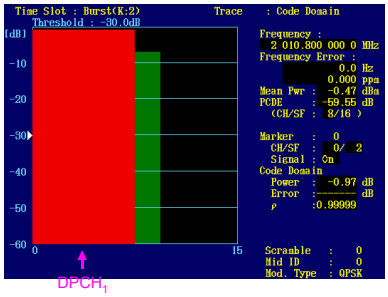


UL RMC 64 kbps

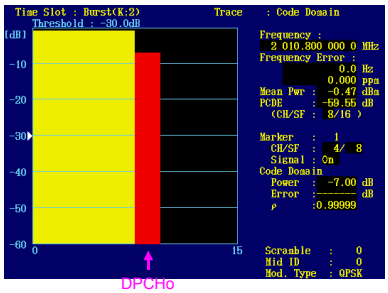


UL RMC 144 kbps

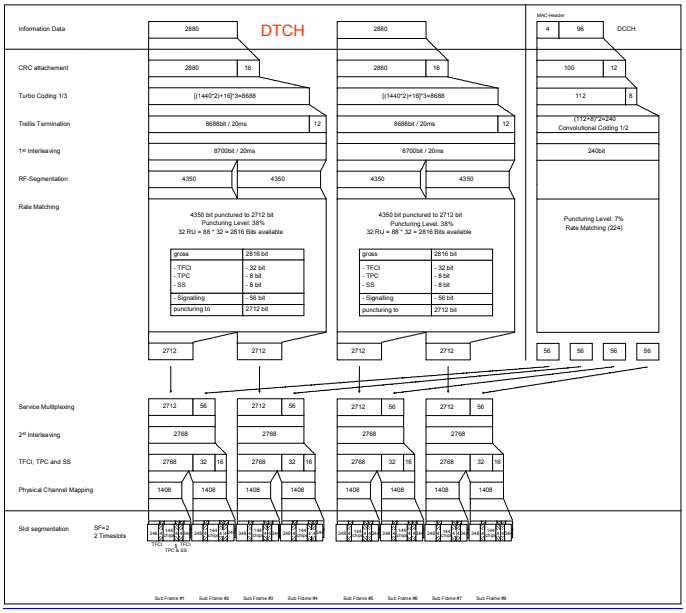




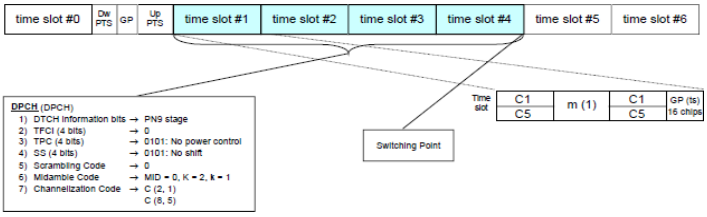
Parameter	Value
Information data rate	12.2 kbps
RU´s allocated	1TS (1*SF8) = 2RU/5ms
Midamble	144
Interleaving	20 ms
Power control	4 Bit/user/10ms
TFCI	16 Bit/user/10ms
Synchronisation Shift (SS)	4 Bit/user/10ms
Inband signalling DCCH	2.4 kbps
Puncturing level at Code rate 1/3 : DCH of the DTCH/ DCH of the DCCH	33% / 33%

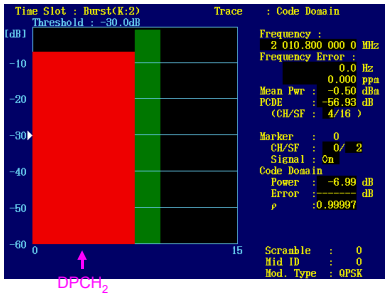


UL RMC 144 kbps

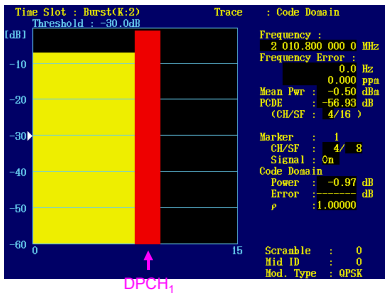


UL RMC 384 kbps

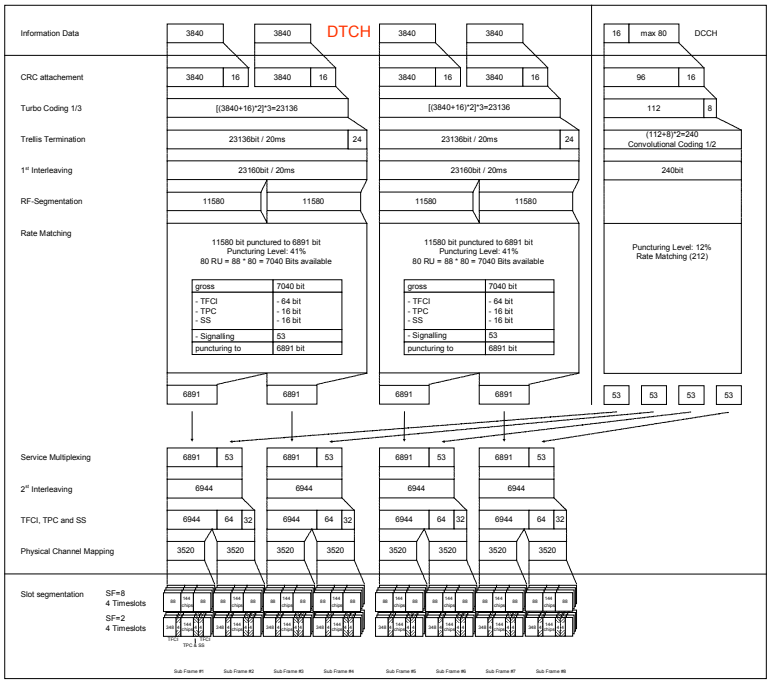




Parameter	Value
Information data rate	384 kbps
RU's allocated	4TS (1*SF2 + 1*SF8) = 40RU/5ms
Midamble	144
Interleaving	20 ms
Power control (TPC)	16 Bit/user/10ms
TFCI	64 Bit/user/10ms
Synchronisation Shift (SS)	16 Bit/user/10ms
Inband signalling DCCH	Max. 2.0 kbps
Puncturing level at Code rate: 1/3 DCH of the DTCH / ½ DCH of the DCCH	41% / 12%



UL RMC 384 kbps

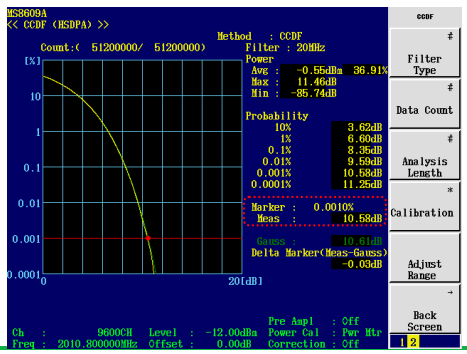


UL RMC Parameters

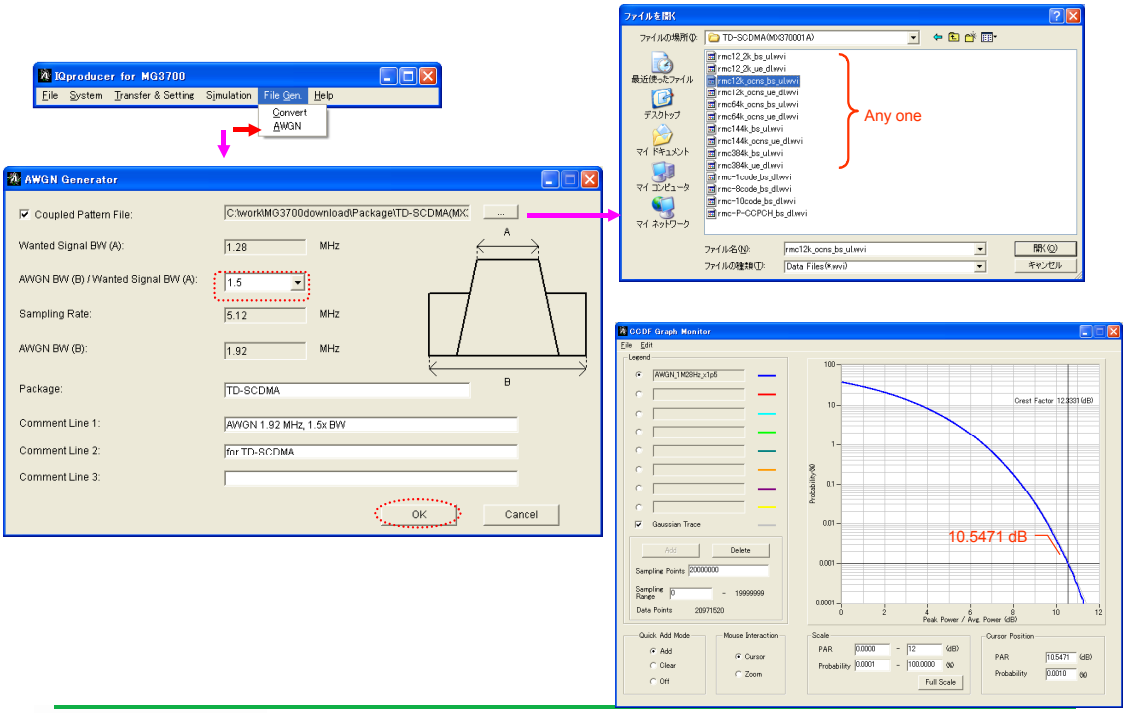
Marker 1	Frame clock
Marker 2	Subframe clock
Marker 3	RF gate
RMS for single phase of IQ	1157
IQ output level	$\sqrt{I^2+Q^2}$ = 320 mV

AWGN

- AWGN (Additive White Gaussian Noise) simulates interference from other cells.
- The minimum bandwidth of the AWGN interferer is 1.5 times the chip rate: 1.92 MHz = 1.5 × 1.28 Mcps
- The flatness across this minimum bandwidth is within ±0.5 dB, and the peak to average ratio at a probability of 0.001% exceeds 10 dB.

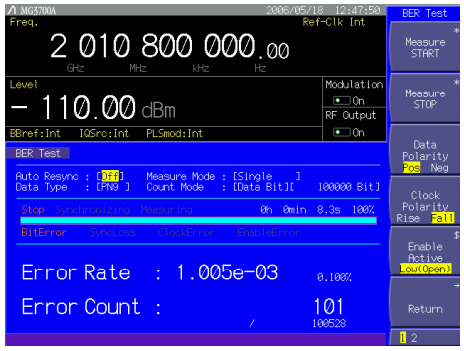


AWGN Setup IQproducer

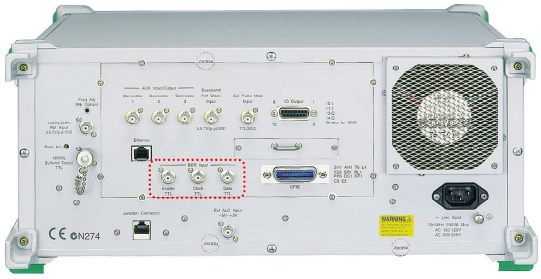


BER Test Setup Example

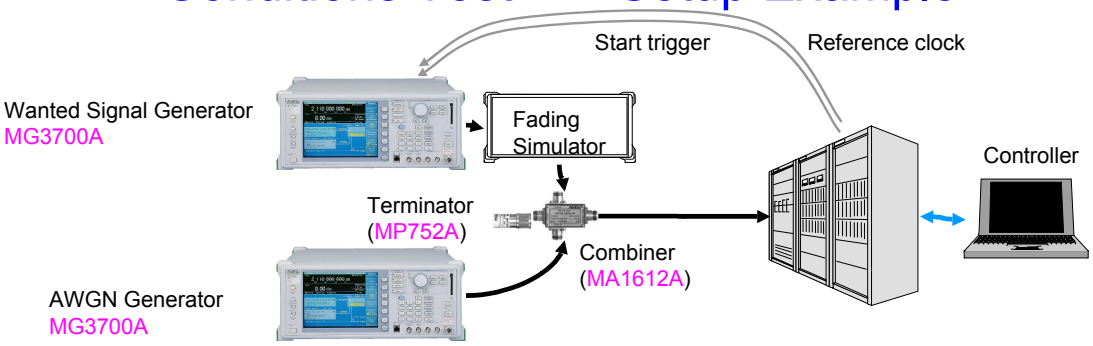
- Received DTCH data
  - » PN9
- Clock
  - » Rise
    - Data
    - Clock
  - » Fall
    - Data
    - Clock



- Measuring bit/time
- Automatic re-synchronization
  - » On
    - – Sync Loss detected
  - » Off
    - – Sync Loss ignored



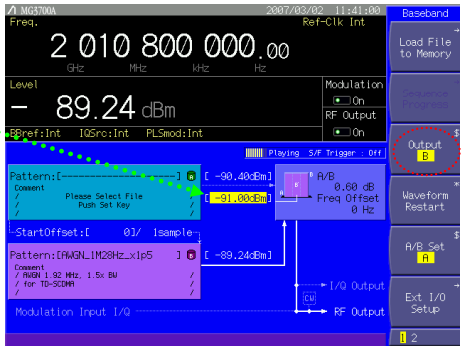
Demodulation of DCH in Multipath Fading Conditions Test Setup Example



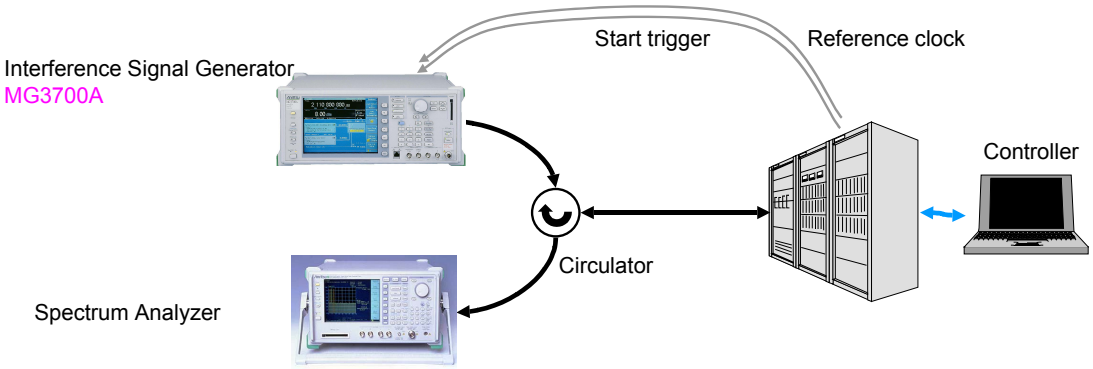
- Start trigger
  - Front panel [Start/Frame Trigger] Input
    - 40 ms × n clock
- Reference clock
  Use only one.
  - Rear panel [Baseband Ref Clock] Input
    - 1.28 MHz, 2 × 1.28 MHz (2.56 MHz), 4 × 1.28 MHz (5.12 MHz)
  - Rear panel [10MHz/5MHz Ref] Input
- Controller
  - Makes receivable state for UL RMC by FTM (Factory Test Mode) control
  - Reports internal BLER calculation for received DTCH

AWGN Setup Example

- AWGN
  - » Ioc [dBm/1.28MHz]



Transmit Intermodulation Test Setup Example



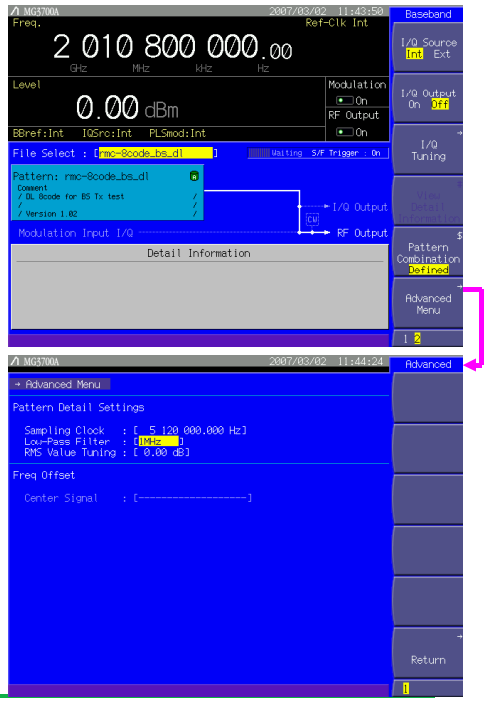
- Start trigger
  - Front panel [Start/Frame Trigger] Input
    - 40 ms × n clock
- Reference clock
  Use only one.
  - Rear panel [Baseband Ref Clock] Input
    - 1.28 MHz, 2 × 1.28 MHz (2.56 MHz), 4 × 1.28 MHz (5.12 MHz)
  - Rear panel [10MHz/5MHz Ref] Input
- Controller
  - Makes maximum transmitting power state by FTM (Factory Test Mode) control

Interference Signal Setup Example

The interference signal is modulated like the BS transmitted signal, and the active time slots of both signals are synchronized.

Table 6.38A: Parameters of the BS transmitted signal for transmit intermodulation testing for 1,28 Mcps TDD

Parameter	Value/description
TDD Duty Cycle	TS i; I = 0, 1, 2, 3, 4, 5, 6: transmit, if i is 0,4,5,6; receive, if i is 1,2,3.
Time slots under test	TS4, TS5 and TS6
BS output power setting	PRAT
Number of DPCH in each time slot under test	8
Power of each DPCH	1/8 of Base Station output power
Data content of DPCH	real life (sufficient irregular)



» Set LPF from Auto (3 MHz) to 1 MHz.
  - To improve ACLR

UE Test

3GPP	TS 25.102 (Release 7)	TS 34.122 (Release 5)	
7	Receiver	6	Receiver
8	Performance requirement	7	Performance requirements
9	Performance requirements (HSDPA)	9	Performance requirements for HSDPA

	Test	Wanted Signal Generator with BERT	Interference Signal Generator	CW Generator	AWGN Generator	Others
7.3	Reference sensitivity level	MG3700A				
7.4	Maximum input level					
7.5	Adjacent Channel Selectivity (ACS)		*			
7.6	Blocking characteristics In-band blocking		*			
	Out of band blocking			MG3692B 20 GHz		MA1612A 3 GHz Combiner
7.7	Spurious response			MG3692B 20 GHz		MA1612A 3 GHz Combiner
7.8	Intermodulation characteristics		*			
8.2	Demodulation in static propagation conditions				*	
8.3	Demodulation of DCH in multi-path fading conditions				MG3700A	MA1612A 3 GHz Combiner Fading simulator
9.2.1	HS-DSCH throughput for Fixed Reference Channels					
9.2.3	Reporting of HS-DSCH Channel Quality Indicator					
9.2.4	HS-SCCH Detection Performance					

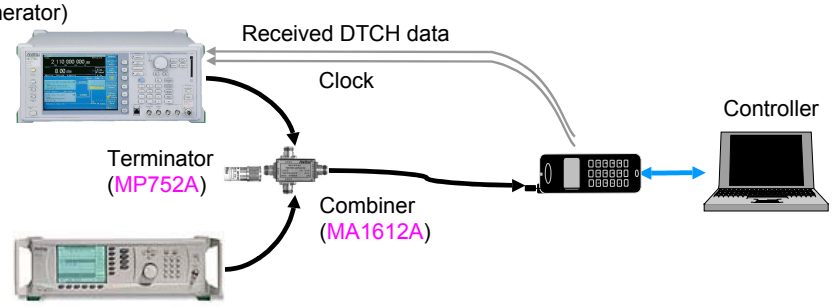
* : MG3700A for the wanted signal generator generates two signals with interference signal, CW or AWGN.

Unsupported interference signal pattern

Unsupported HSPA

Receiver Test Setup Example

Wanted Signal Generator
(+ Interference Signal Generator)
(+ CW Generator)
(+ AWGN Generator)
BER Tester
MG3700A



– Controller
  - Makes receivable state for DL RMC by FTM (Factory Test Mode) control
  - Reports internal BLER calculation for received DTCH

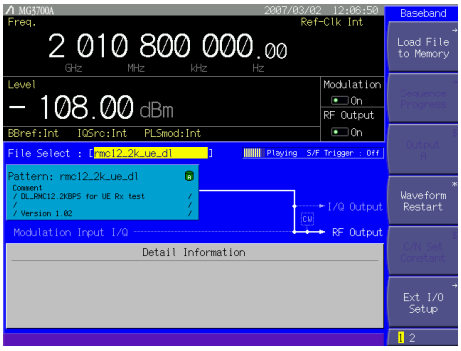
Scrambling Code Synchronization Setup Example

- Scrambling code
  - » Each basic midamble code is associated with a cell-specific complex scrambling code.
    - – Created from 16-bit long complex scrambling sequences
  - » Applies to scrambling (spreading)
- Set the scrambling code and basic midamble code to UE.
  - – 0

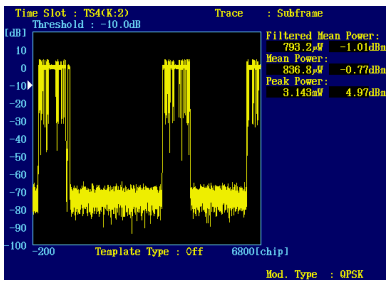
Code Group	Associated Codes			
	SYNC-DL ID	SYNC-UL ID	Scrambling Code ID	Basic Midamble Code ID
Group 1	0	0...7	0	0
			1	1
			2	2
			3	3
Group 2	1	8...15	4	4
			5	5
			6	6
			7	7
			.	
			.	
			.	
Group 32	31	248...255	124	124
			125	125
			126	126
			127	127

Wanted Signal Setup Example

Test
- – Receiver
  excluding
  Maximum input level
- DL RMC 12.2 kbps



Setting power level is the Mean power.



Mean power is the power in a bandwidth of at least (1+α) times 1.28 MHz chip rate. The measurement period is a transmit timeslot excluding the guard period.

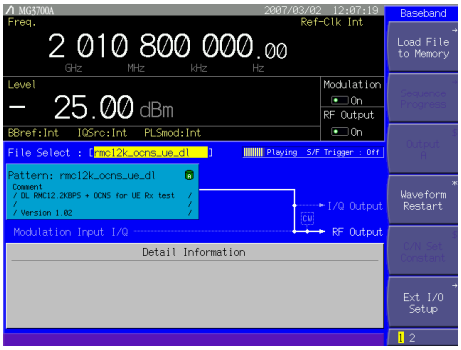
RRC filtered mean power is the power measured through a root raised cosine filter with roll-off α=0.22 and 1.28 MHz chip rate bandwidth.

For a perfectly modulated signal,
RRC filtered mean power = Mean power - 0.246 dB

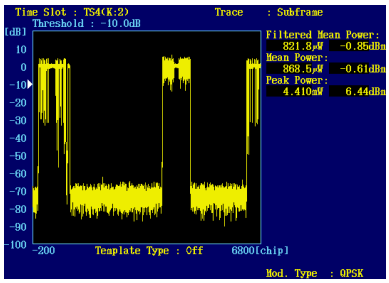
Wanted Signal Setup Example

Test
- Maximum input level

- DL RMC 12.2 kbps
  - DPCHo multiplexing



Setting power level is the Mean power.



Mean power is the power in a bandwidth of at least (1+α) times 1.28 MHz chip rate. The measurement period is a transmit timeslot excluding the guard period.

RRC filtered mean power is the power measured through a root raised cosine filter with roll-off α=0.22 and 1.28 MHz chip rate bandwidth.

For a perfectly modulated signal,
RRC filtered mean power = Mean power - 0.246 dB

Wanted Signal + Interference Signal Setup Example

Test
- ACS
- Blocking characteristics
- Intermodulation characteristics

- DL RMC 12.2 kbps
  +
- Interferer
  - » Set Frequency offset
    - -31.9872 ~ +31.9872 MHz

ACS: 1.6 MHz offset
Blocking: 3.2 & 4.8 MHz offset
Intermodulation: 6.4 MHz offset

Unsupported interference signal pattern

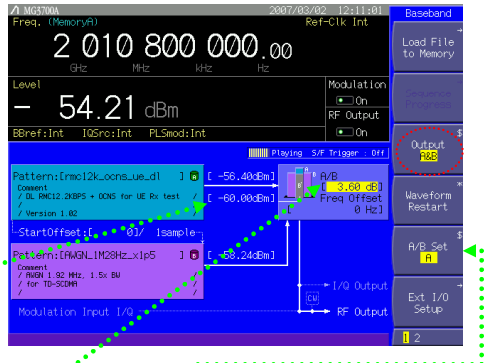
Interference Signal

The Interference signal is equivalent to a continuous wideband CDMA signal with one code of chip frequency 1.28 Mcps, filtered by an RRC transmit pulse-shaping filter with roll-off α = 0.22.

Wanted Signal + AWGN Setup Example

Test
– Performance requirements

- DL RMC 12.2 kbps
  – DPCHo multiplexing
- DL RMC 64 kbps
  – DPCHo multiplexing
- DL RMC 144 kbps
  – DPCHo multiplexing
- DL RMC 384 kbps
  +
- AWGN
  » Ioc [dBm/1.28MHz]



A/B Set	A level	B level	RF level
A	Variable	Static	Coupled
B	Static	Variable	Coupled
Constant	Variable	Variable	Static

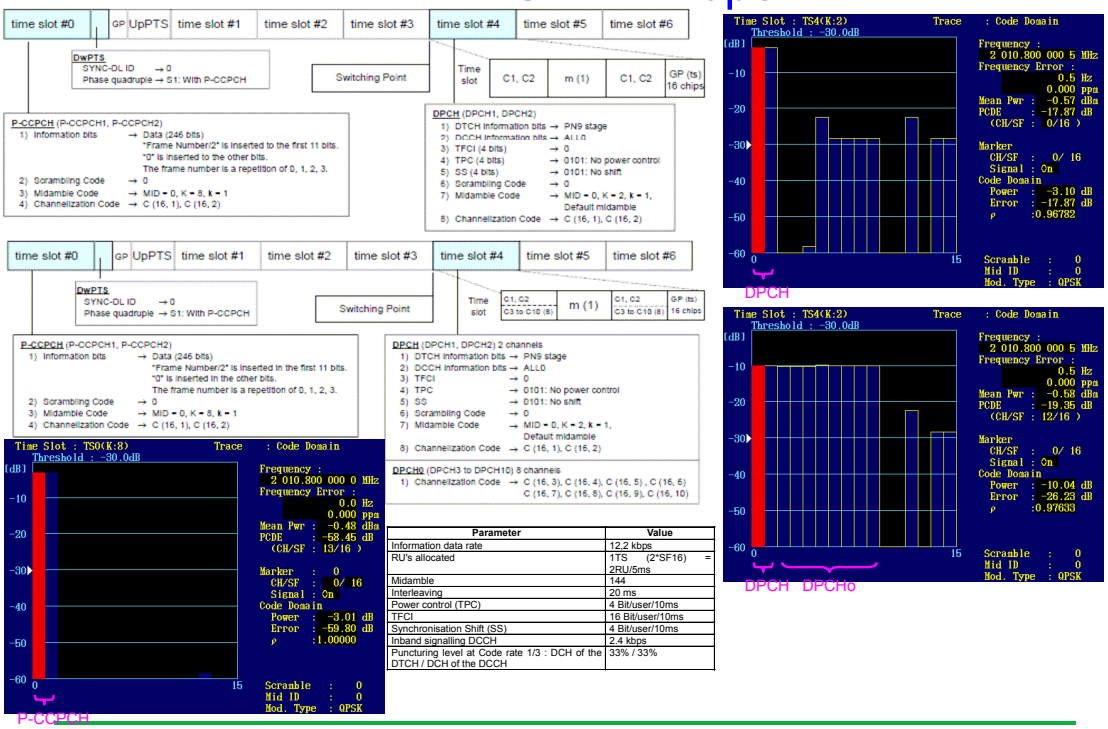
Test Number	$\frac{\hat{I}_{or}}{I_{oc}}$ [dB]	BLER
1	3.6	10^{-2}
2	2.4	10^{-1}
	2.7	10^{-2}
3	2.8	10^{-1}
	3.2	10^{-2}
4	3.2	10^{-1}

DPCHo

DPCHo simulates an individual intra-cell interferer that is equivalent to a valid UTRA TDD signal with SF 16, using the same time slot(s) as the wanted signal and applying the same cell-specific scrambling code.

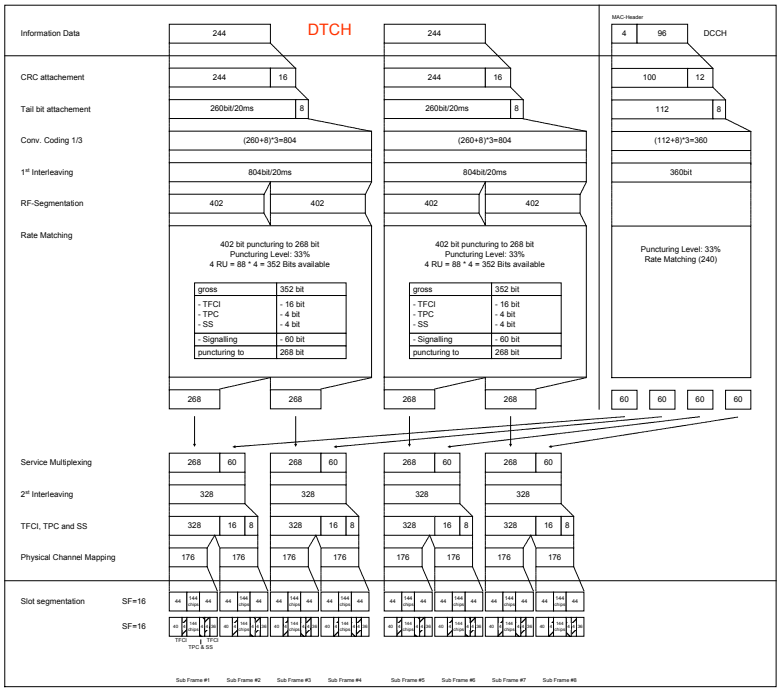
Parameters	Unit	Test 1	Test 2	Test 3	Test 4
Number of $DPCH_o$		8	2	2	0
Scrambling code and basic midamble code number (see note)		0	0	0	0
DPCH Channelization Codes (see note)	C(k,Q)	C(i,16) i=1,2	C(i,16) i=1…8	C(i,16) i=1…8	C(i,16) i=1…10
$DPCH_o$ Channelization Codes (see note)	C(k,Q)	C(i,16) 3≤ i ≤10	C(i,16) 9≤ i ≤10	C(i,16) 9≤ i ≤10	-
$\frac{DPCH_o\_E_c}{I_{or}}$	DB	-10	-10	-10	0
I_{oc}	dBm/1,28MHz	-60			
Information Data Rate	Kbps	12.2	64	144	384

DL RMC 12.2 kbps

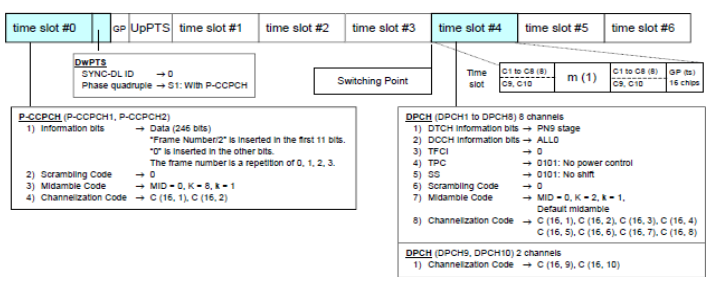


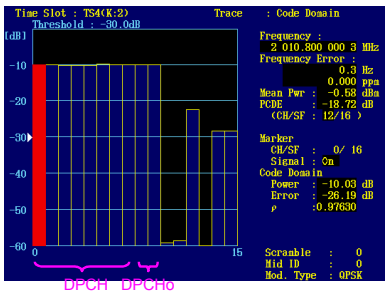
Parameter	Value
Information data rate	12.2 kbps
RU's allocated	1TS (2*SF16) = 2RU/5ms
Midamble	144
Interleaving	20 ms
Power control (TPC)	4 Bit/user/10ms
TFCI	16 Bit/user/10ms
Synchronisation Shift (SS)	4 Bit/user/10ms
Inband signalling DCCH	2.4 kbps
Puncturing level at Code rate 1/3 : DCH of the DTCH / DCH of the DCCH	33% / 33%

DL RMC 12.2 kbps



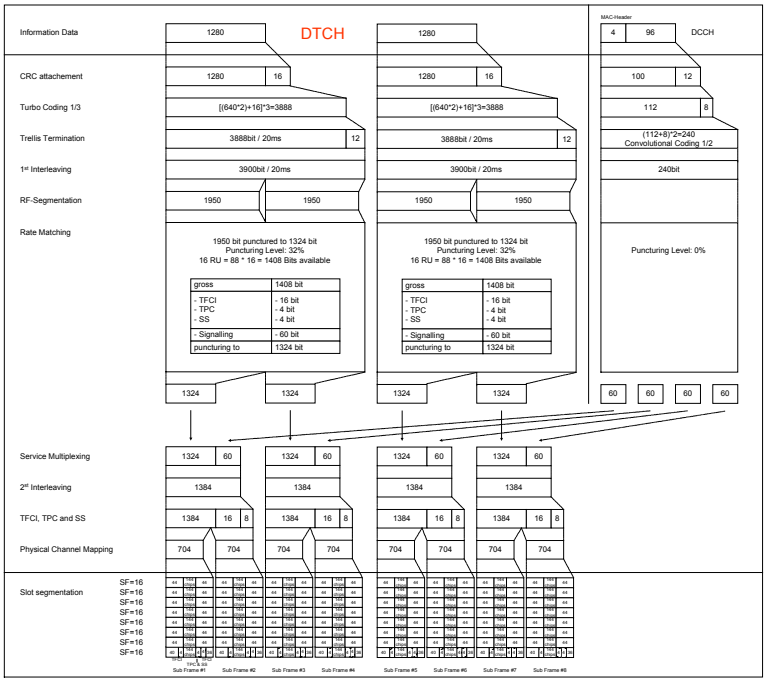
DL RMC 64 kbps



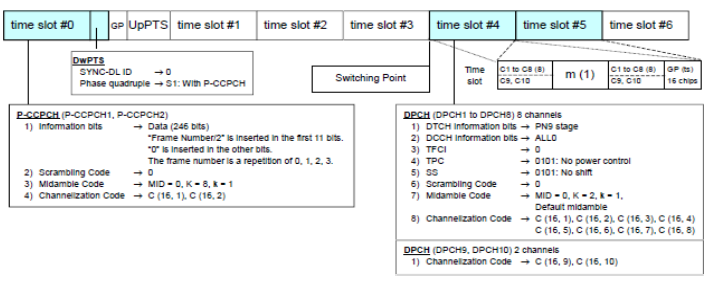


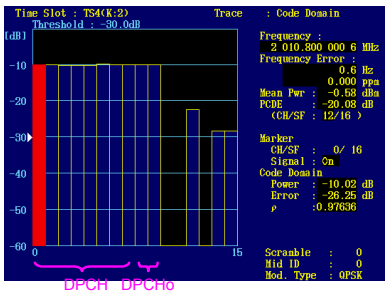
Parameter	Value
Information data rate	64 kbps
RU's allocated	1TS (8*SF16) = 8RU/5ms
Midamble	144
Interleaving	20 ms
Power control (TPC)	4 Bit/user/10ms
TFCI	16 Bit/user/10ms
Synchronisation Shift (SS)	4 Bit/user/10ms
Inband signalling DCCH	2.4 kbps
Puncturing level at Code rate: 1/3 DCH of the DTCH/ ½ DCH of the DCCH	32% / 0

DL RMC 64 kbps



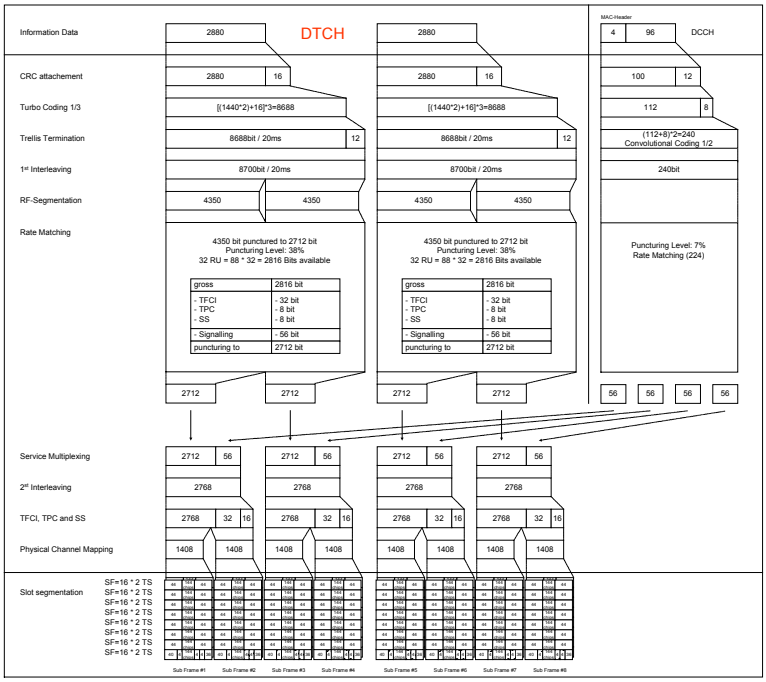
DL RMC 144 kbps



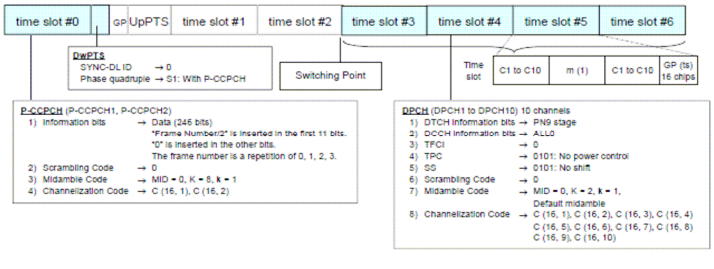


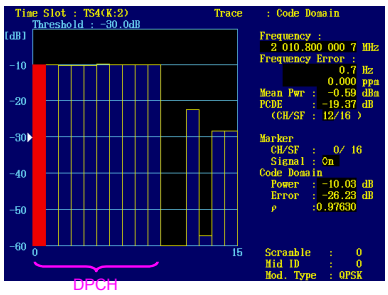
Parameter	Value
Information data rate	144 kbps
RU's allocated	2TS (8*SF16) = 16RU/5ms
Midamble	144
Interleaving	20 ms
Power control (TPC)	8 Bit/user/10ms
TFCI	32 Bit/user/10ms
Synchronisation Shift (SS)	8 Bit/user/10ms
Inband signalling DCCH	2.4 kbps
Puncturing level at Code rate: 1/3 DCH of the DTCH/ ½ DCH of the DCCH	38% / 7%

DL RMC 144 kbps



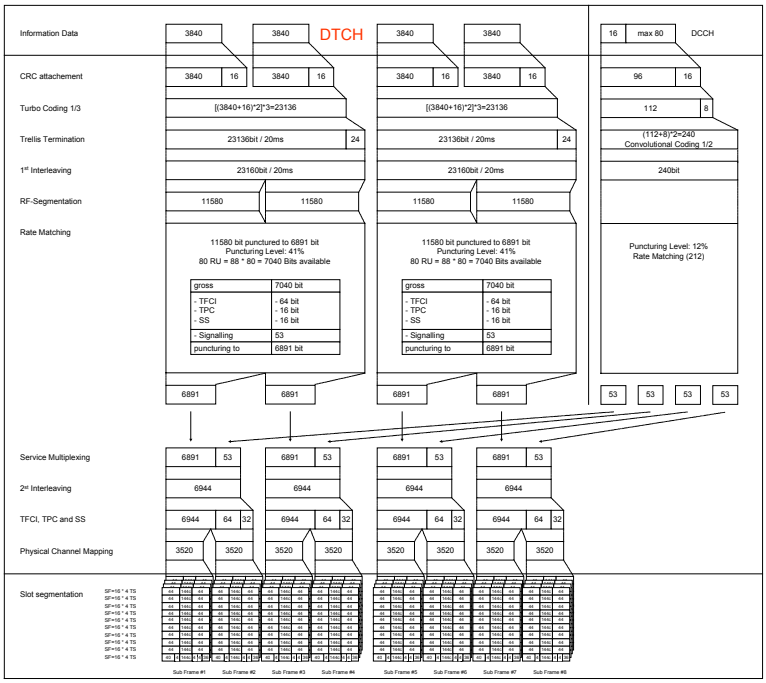
DL RMC 384 kbps





Parameter	Value
Information data rate	384 kbps
RU's allocated	4TS (10*SF16) = 40RU/5ms
Midamble	144
Interleaving	20 ms
Power control (TPC)	16 Bit/user/10ms
TFCI	64 Bit/user/10ms
Synchronisation Shift (SS)	16 Bit/user/10ms
Inband signalling DCCH	max.2 kbps
Puncturing level at Code rate: 1/3 DCH of the DTCH/ ½ DCH of the DCCH	41% / 12%

DL RMC 384 kbps

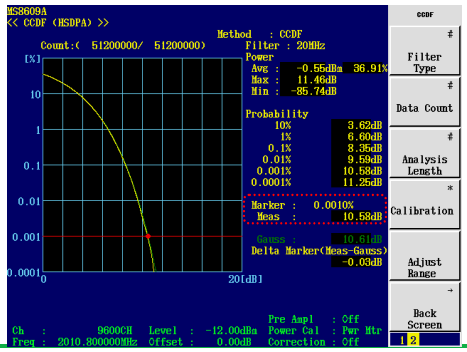


DL RMC Parameters

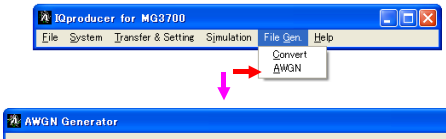
Marker 1	Frame clock
Marker 2	Subframe clock
Marker 3	RF gate
RMS for single phase of IQ	1157
IQ output level	$\sqrt{I^2+Q^2}$ = 320 mV

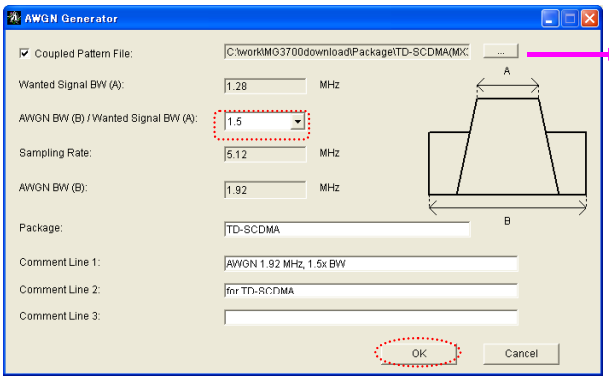
AWGN

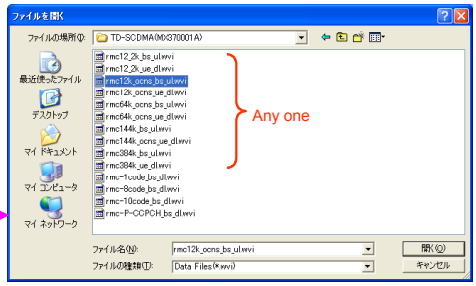
- AWGN (Additive White Gaussian Noise) simulates interference from other cells.
- The minimum bandwidth of the AWGN interferer is 1.5 times the chip rate (1.92 MHz = 1.5 × 1.28 Mcps).
- The flatness across this minimum bandwidth is within ±0.5 dB, and the peak to average ratio at a probability of 0.001% exceeds 10 dB.

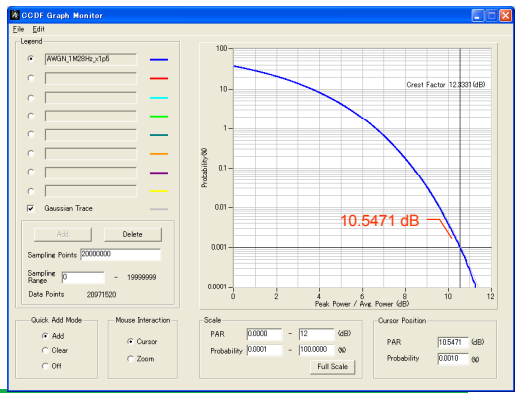


AWGN Setup IQproducer



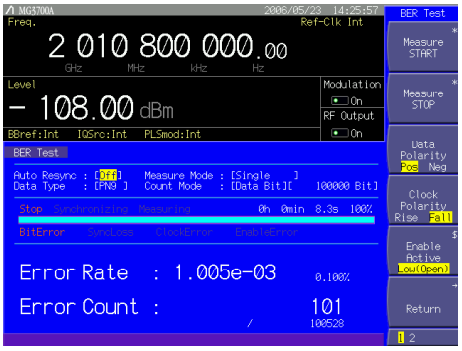




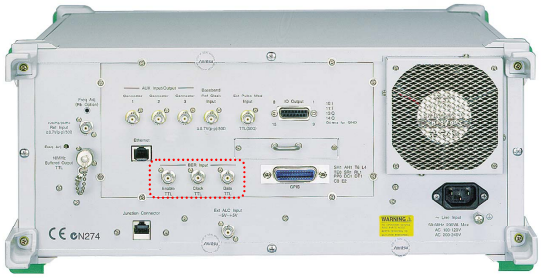


BER Test Setup Example

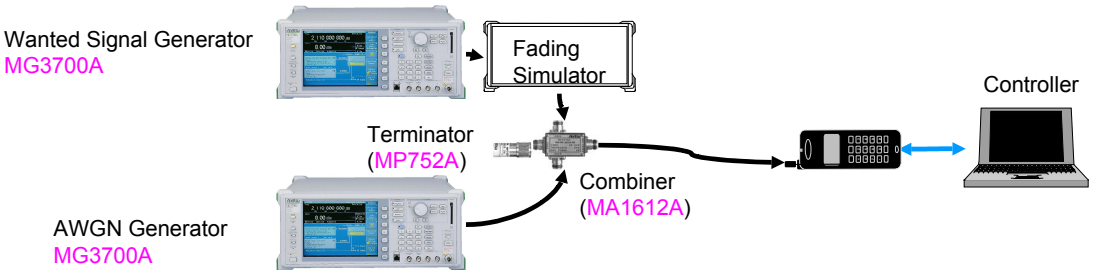
- Received DTCH data
  - » PN9
- Clock
  - » Rise
    - Data
    - Clock
  - » Fall
    - Data
    - Clock



- Measuring bit/time
- Automatic re-synchronization
  - » On
    - – Sync Loss detected
  - » Off
    - – Sync Loss ignored



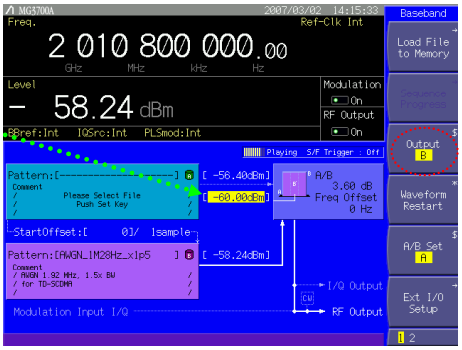
Demodulation of DCH in Multipath Fading Conditions Test Setup Example



- – Controller
  - Makes receivable state for DL RMC by FTM (Factory Test Mode) control
  - Reports internal BLER calculation for received DTCH

AWGN Setup Example

- AWGN
  - » Ioc [dBm/1.28MHz]

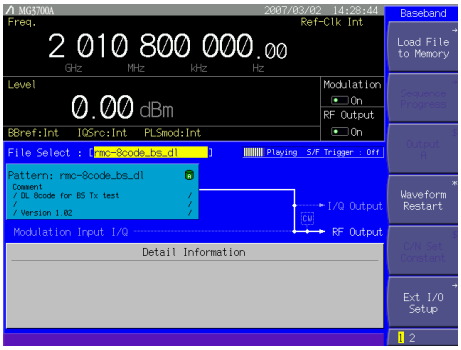


Additional Information

- BS Transmitted Signal for BS Transmitter Test 75
  - – Explore 3GPP TS 25.142
- UL RMC for UE Transmitter Test 89
  - – Explore 3GPP TS 34.122

BS Transmitted Signal for BS Transmitter Test

Test
- Maximum output power
- Transmit ON/OFF time mask
- OBW
- Spectrum emission mask
- ACLR
- Spurious emissions
- Transmit intermodulation

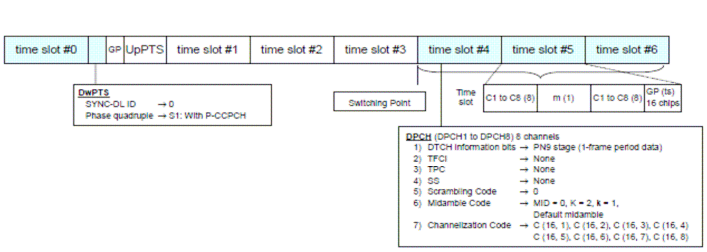


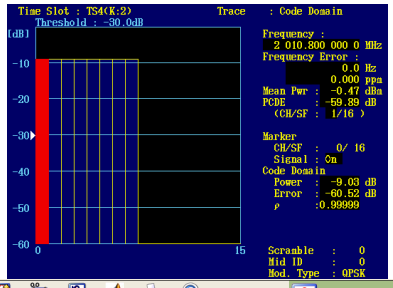
- DL 8 DPCH

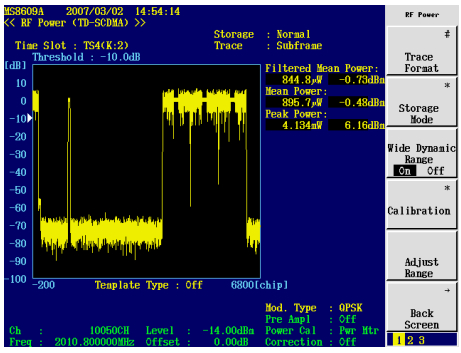
Parameter	Value/description
TDD Duty Cycle	TS i; i = 0, 1, 2, 3, 4, 5, 6: transmit, if i is 0,4,5,6; receive, if i is 1,2,3.
Time slots under test	TS4, TS5 and TS6
BS output power setting	PRAT
Number of DPCH in each time slot under test	8
Power of each DPCH	1/8 of Base Station output power
Data content of DPCH	real life (sufficient irregular)

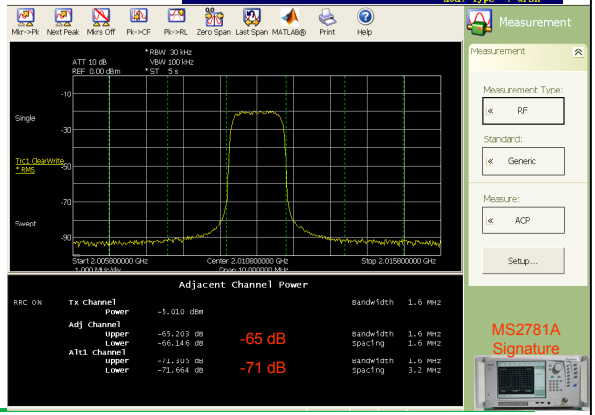
PRAT: Rated output power of BS
It is the mean power level per carrier that the manufacturer has declared to be available at the antenna connector.

DL 8 DPCH



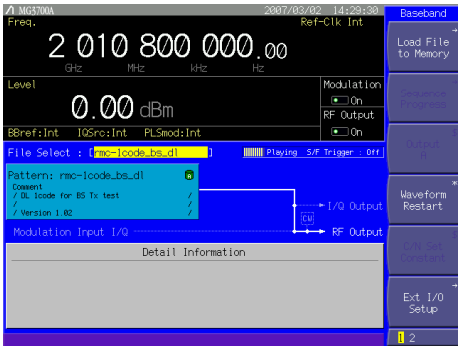






BS Transmitted Signal for BS Transmitter Test

Test
- Frequency stability
- Minimum output power
- EVM (at Pmax –30 dB)

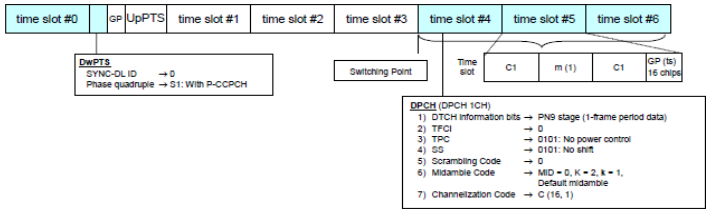


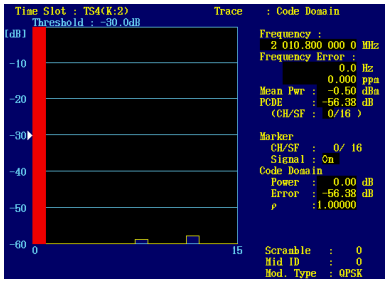
- DL 1 DPCH

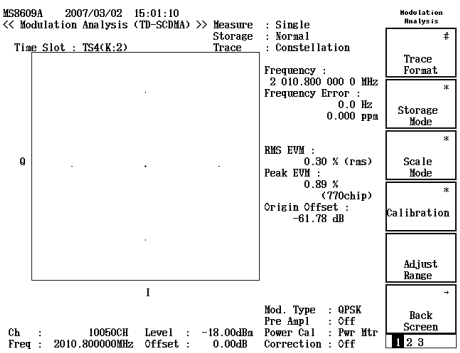
Parameter	Value/description
TDD Duty Cycle	TS i; i = 0, 1, 2, ..., 6: transmit, if i is 0, 4,5,6; receive, if i is 1,2,3.
Time slots under test	TS4, TS5 and TS6
Number of DPCH in eachtime slot under test	1
BS output power setting	PRAT
Data content of DPCH	real life (sufficient irregular)

PRAT: Rated output power of BS
It is the mean power level per carrier that the manufacturer has declared to be available at the antenna connector.

DL 1 DPCH





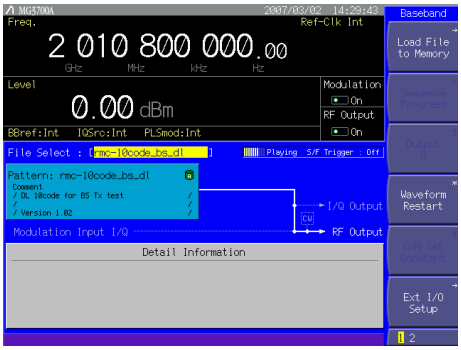


BS Transmitted Signal for BS Transmitter Test

Test
- EVM
- PCDE

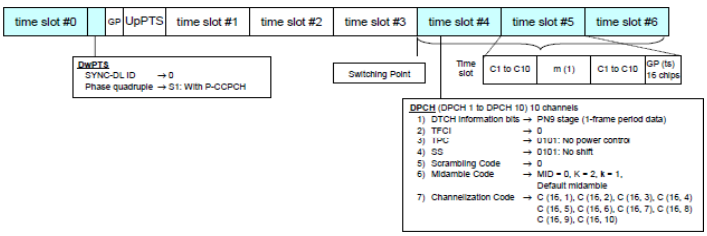
- DL 10 DPCH

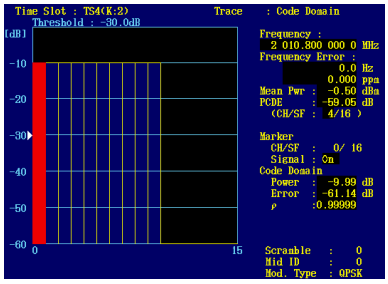
Parameter	Value/description
TDD Duty Cycle	TS i; i = 0, 1, 2, ..., 6: transmit, if i is 0,4,5,6; receive, if i is 1,2,3.
Time slots under test	TS4, TS5 and TS6
BS output power setting	PRAT
Number of DPCH in each time slot under test	10
Power of each DPCH	1/10 of Base Station output power
Data content of DPCH	real life (sufficient irregular)
Spreading factor	16

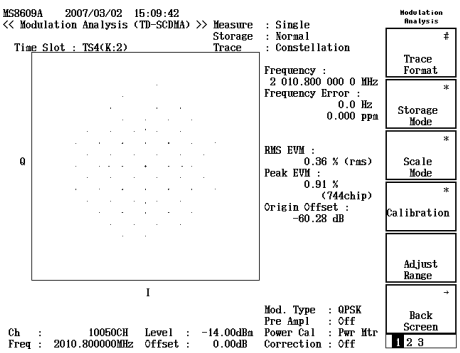


PRAT: Rated output power of BS
It is the mean power level per carrier that the manufacturer has declared to be available at the antenna connector.

DL 10 DPCH





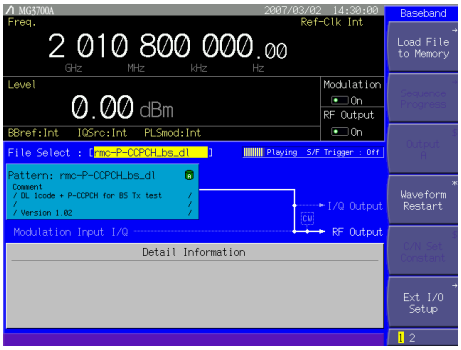


BS Transmitted Signal for BS Transmitter Test

Test
- P-CCPCH power
- Differential accuracy of P-CCPCH power

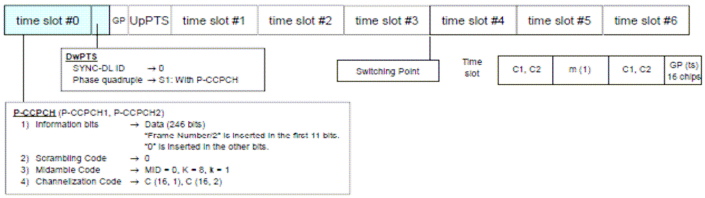
- DL P-CCPCH

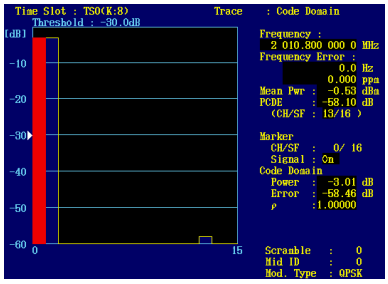
Parameter	Value/description
TDD Duty Cycle	TS i; i = 0, 1, 2, ..., 6: transmit, if i is 0,4,5,6; receive, if i is 1,2,3.
Time slots carrying PCCPCH	TS 0
BS output power setting	PRAT
Relative power of PCCPCH	½ of BS output power
Data content of DPCH	real life (sufficient irregular)

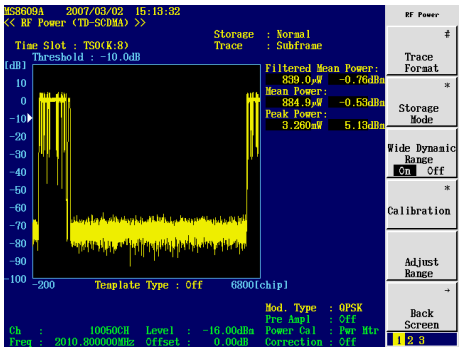


PRAT: Rated output power of BS
It is the mean power level per carrier that the manufacturer has declared to be available at the antenna connector.

DL P-CCPCH







BS Transmitted Signal for BS Transmitter Test

Test
- Spectrum emission mask
- ACLR
- Spurious emissions
- Transmit intermodulation
- EVM
- PCDE

Unsupported HSPA

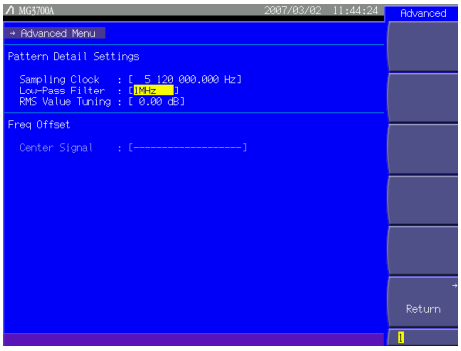
- DL 8 HS-PDSCH

Parameter	Value/description
TDD Duty Cycle	TS i; i = 0, 1, 2, 3, 4, 5, 6: transmit, if i is 0,4,5,6; receive, if i is 1,2,3.
Time slots under test	TS4, TS5 and TS6
BS output power setting	PRAT
HS-PDSCH modulation	16QAM
Number of HS-PDSCH in each time slot under test	8
Power of each HS-PDSCH	1/8 of Base Station output power
Data content of HS-PDSCH	real life (sufficient irregular)
Spreading factor	16

PRAT: Rated output power of BS
It is the mean power level per carrier that the manufacturer has declared to be available at the antenna connector.

BS Transmitted Signal for BS Transmitter Test

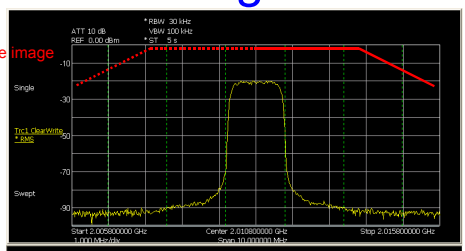
» Set LPF properly.
- To improve ACLR



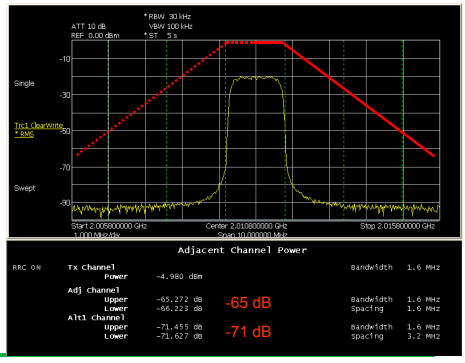
Effect of ACLR on LPF Setting

- DL 8 DPCH

LPF curve image

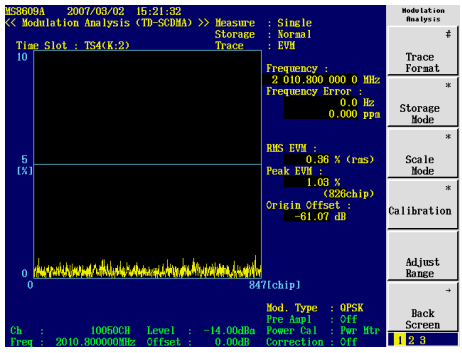


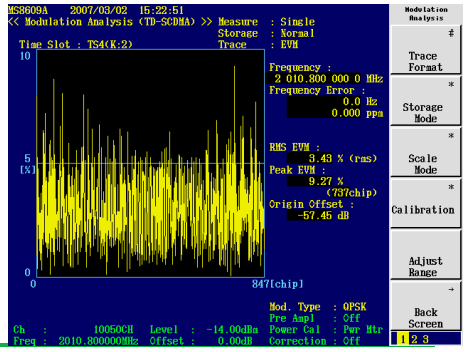
» When LPF changed from Auto (3 MHz) to 1 MHz



Effect of EVM on LPF Setting

- DL 10 DPCH



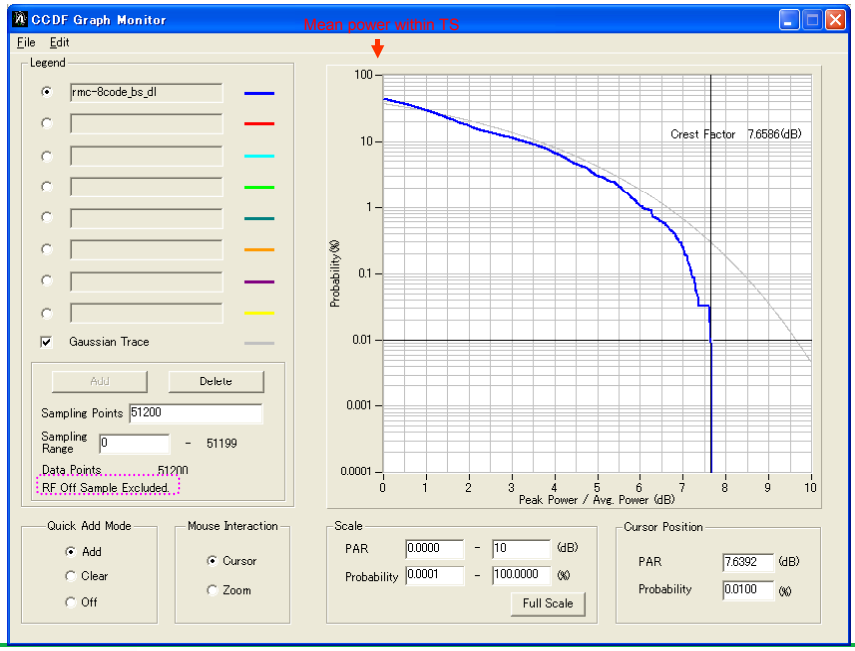


» When LPF changed from Auto (3 MHz) to 1 MHz

BS Transmitted Signal for BS Transmitter Test Parameters

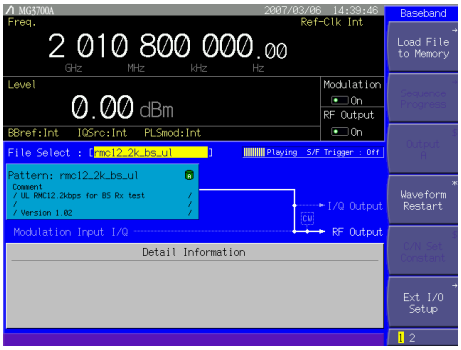
Marker 1	Frame clock
Marker 2	Subframe clock
Marker 3	RF gate
RMS for single phase of IQ	1157
IQ output level	$\sqrt{I^2+Q^2}$ = 320 mV

BS Transmitted Signal for BS Transmitter Test CCDF Simulation



UL RMC for UE Transmitter Test

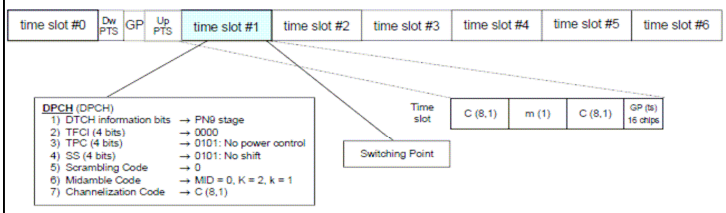
Test
- Maximum output power
- Frequency stability
- Minimum output power
- Transmit ON/OFF time mask
- OBW
- Spectrum emission mask
- ACLR
- Spurious emissions
- Transmit intermodulation
- EVM

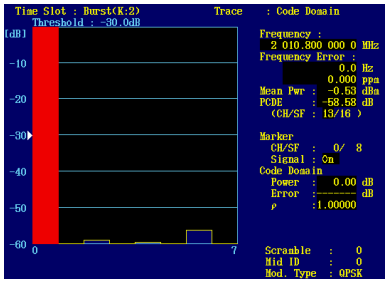


- UL RMC 12.2 kbps

Parameter	Value/description
UL Reference measurement channel	12,2kbps, according to annex C.2.1
Uplink Power Control	SS level and signalling values such that UE transmits maximum power.
Data content	real life (sufficient irregular)

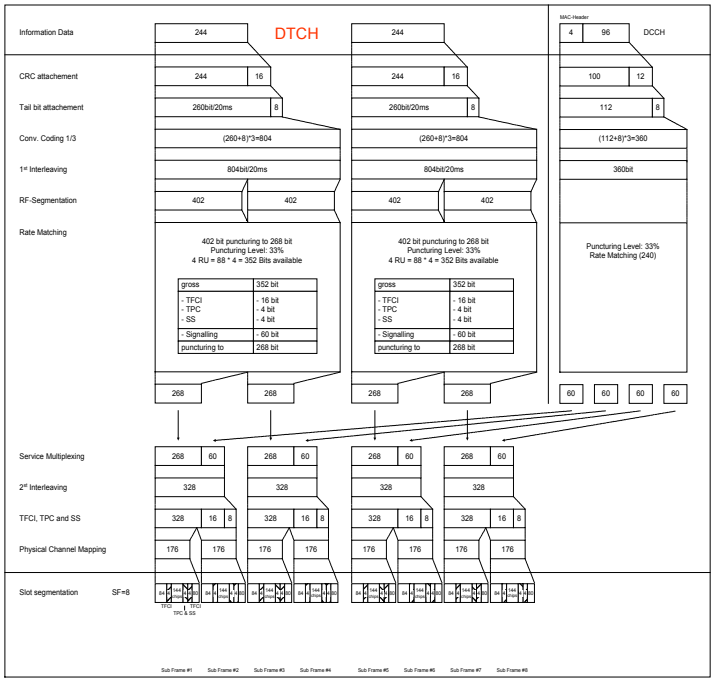
UL RMC 12.2 kbps



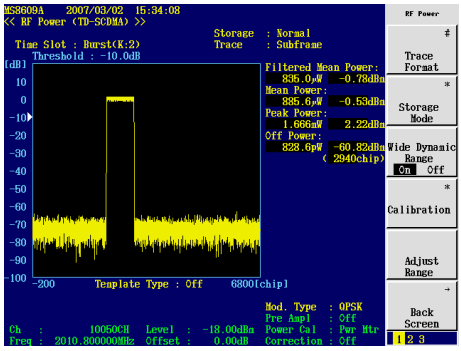


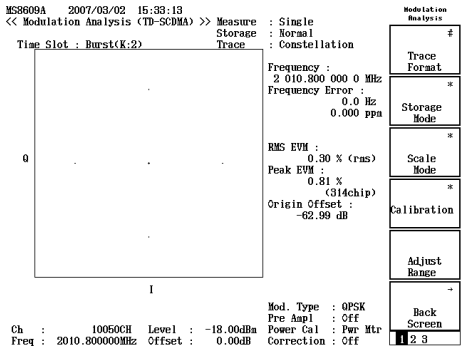
Parameter	
Information data rate	12,2 kbps
RU's allocated	1TS (1*SF8) = 2RU/5ms
Midamble	144
Interleaving	20 ms
Power control (TPC)	4 Bit/user/10ms
TFCI	16 Bit/user/10ms
Synchronisation Shift (SS)	4 Bit/user/10ms
Inband signalling DCCH	2 kbps
Puncturing level at Code rate 1/3: DCH of the DTCH / DCH of the DCCH	33% / 33%

UL RMC 12.2 kbps



UL RMC 12.2 kbps





UL RMC for UE Transmitter Test

Test
- Maximum output power
- PCDE

- UL RMC multicode 12.2 kbps

Unsupported signal pattern

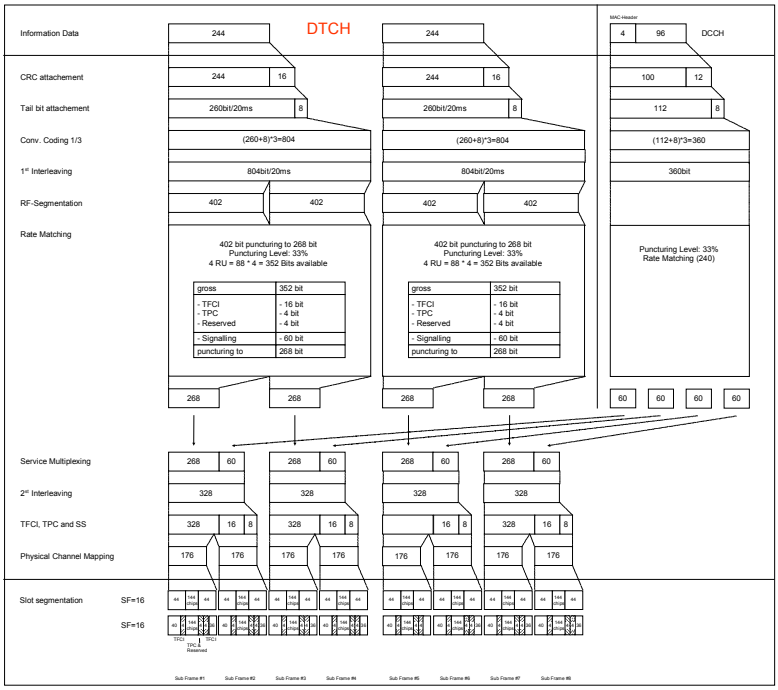
Parameter	Value/description
Reference measurement channel	Multicode 12,2 kbps, according to annex C.2.2.2
Uplink Power Control	SS level and signalling values such that UE transmits maximum power
Data content	real life (sufficient irregular)

UL RMC Multicode 12.2 kbps

Unsupported signal pattern

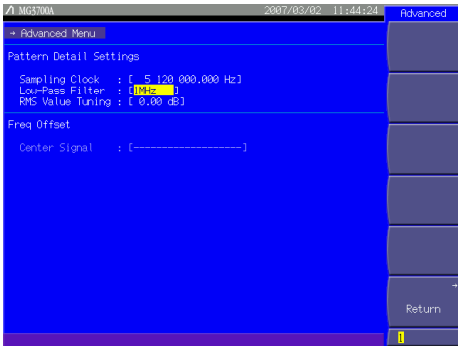
Parameter	Value
Information data rate	12,2 kbps
RU's allocated	1TS (2*SF16) = 2RU/5ms
Midamble	144
Interleaving	20 ms
Power control (TPC)	4 Bit/user/10ms
TFCI	16 Bit/user/10ms
4 Bit reserved for future use (place of SS)	4 Bit/user/10ms
Inband signalling DCCH	2.4 kbps
Puncturing level at Code rate 1/3: DCH of the DTCH / DCH of the DCCH	33% / 33%

UL RMC Multicode 12.2 kbps



UL RMC for UE Transmitter Test

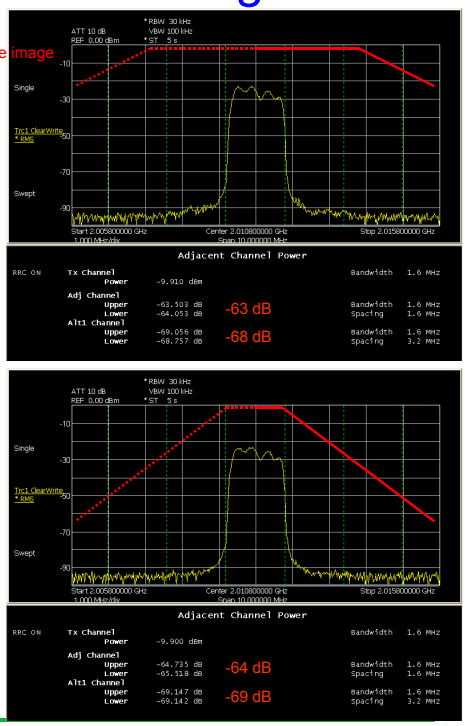
» Set LPF properly.
  – To improve ACLR



Effect of ACLR on LPF Setting

- UL RMC 12.2 kbps

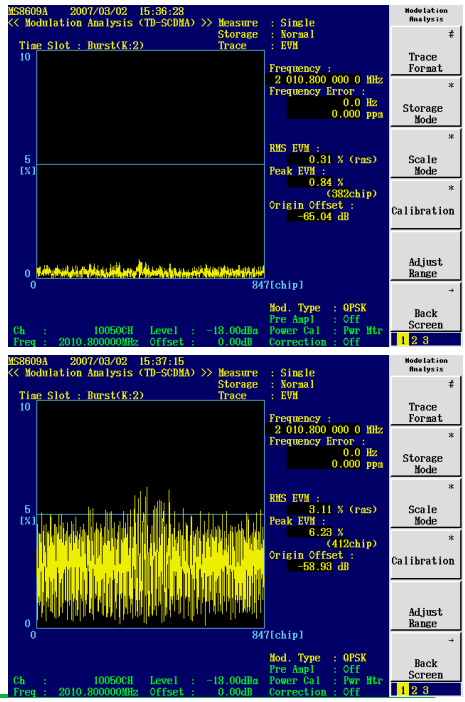
LPF curve image



» When LPF changed from Auto (3 MHz) to 1 MHz

Effect of EVM on LPF Setting

- UL RMC 12.2 kbps

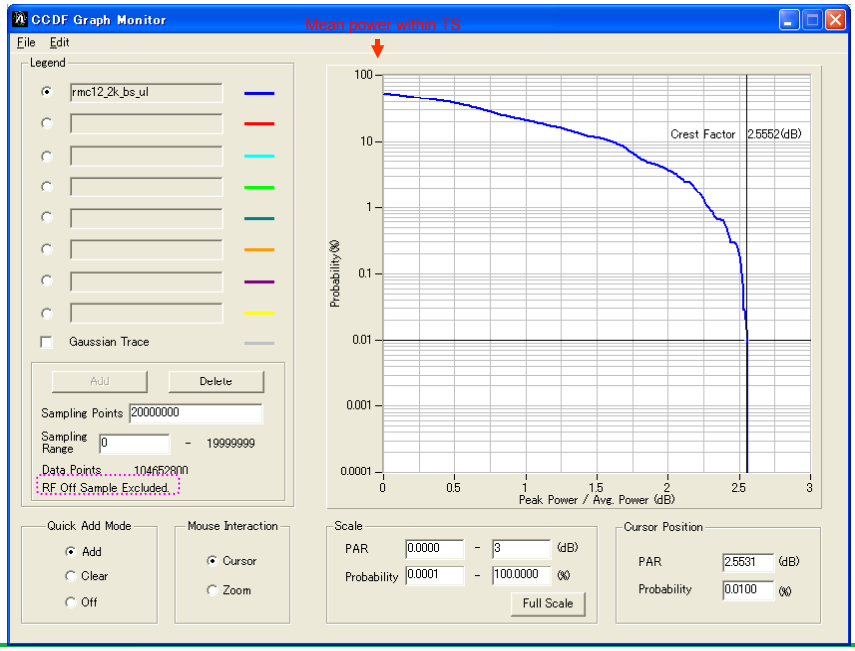


» When LPF changed from Auto (3 MHz) to 1 MHz

UL RMC for UE Transmitter Test Parameters

Marker 1	Frame clock
Marker 2	Subframe clock
Marker 3	RF gate
RMS for single phase of IQ	1157
IQ output level	$\sqrt{I^2+Q^2}$ = 320 mV

UL RMC for UE Transmitter Test CCDF Simulation



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